TUTORIAL: Linking the Veritools PLI

This tutorial describes how to link the Veritools PLI with your simulator.

General

Users link in the Veritools PLI routine to run their Verilog simulator and produce very compressed/optimized files. It also allows users to run their simulator with Undertow Suite in an interactive mode. The Veritools PLI routine typically outputs files compressed by a factor of 600-900 times smaller than the equivalent VCD data and accelerates the simulation time by a factor of 4-5 times.

Users can link in the Veritools PLI dynamically so that no compile operation is required. When the simulator is running, the dynamic link will automatically link the users's simulator to the Veritools PLI and output the compressed files and/or connect to the Undertow Suite program.

Step 1: Link the Veritools PLI Routine to your Simulator dynamically

First set the UT_ROOT_DIR environment variable to your Undertow distribution directory location.

```
% setenv  UT_ROOT_DIR /yourpath
```

Link with Model Tech

```
% setenv  PLIOBJS  $UT_ROOT_DIR/PLI/vtpli_modtech.so
```

Link with Verilog XL

Option 1:

```
%setenv  LD_LIBRARY_PATH  ${LD_LIBRARY_PATH}:${UT_ROOT_DIR}/PLI
```

Option 2: add the following to your command line

```
+loadpli1=$(UT_ROOT_DIR)/PLI/libpli.so:my_bootstrap
```

Link with NC Verilog

Option 1:

```
%setenv  LD_LIBRARY_PATH  ${LD_LIBRARY_PATH}:${UT_ROOT_DIR}/PLI
```

Option 2: add the following to your command line

```
+loadpli1=$(UT_ROOT_DIR)/PLI/libpli.so:my_bootstrap
```

Link with VCS

1. Batch Mode

```
% vcs +cli +acc+4 -Mupdate top.v iv.v $UT_ROOT_DIR/PLI/vtplivcs.o -P $UT_ROOT_DIR/PLI/vt_vcs.tab -lm
```

2. Interactive Mode

```
% vcs +cli +acc+4 -line -Mupdate top.v iv.v $UT_ROOT_DIR/PLI/vtplivcs.o -P $UT_ROOT_DIR/PLI/vt_vcs.tab -lm
```

STEP 2: Add the command line into your Verilog source code in order to dump your waveform files:

Initiate your simulator to run the Veritools PLI by adding the system command "$vtDumpvars;" to your Verilog source code. This command can replace the "$dumpvars;" and is usually placed close to the top of your source files:

```
initial
  begin
        $vtDumpvars;
  end
```

STEP 3: Add a line to your Verilog command line to specify the amount of compression you want:

+VTCOMPRESS20	(20-40 x compression)
+VTCOMPRESS200	(40-60 x compression)
+VTCOMPRESS250	(600-900 x compression)

```
% filename_ver -f verilogFile +VTCOMPRESS250
```

Veritools

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