Veritools

Undertow Tutorial

Veritools

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Undertow Digital
Basic Features

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Set the license environment variables

- Root directory
  setenv UT_ROOT_DIR *<path to Undertow distribution>*
- Work directory
  setenv UT_WORK_DIR *<path to desired work directory>*
- License file
  setenv LM_LICENSE_FILE *flexlm/license.dat*
- Display*
  setenv DISPLAY *<machine id>*
  Only if Undertow distribution resides in another machine
- Navigate to the directory containing Undertow distribution and on the command line
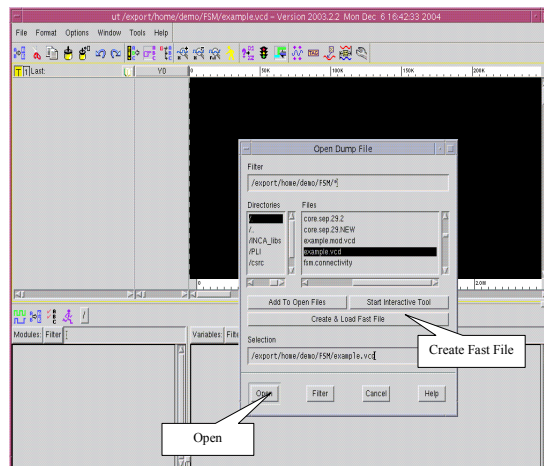 type   ./ut

Veritools

Mouse Operations

- Select or click - use *left* mouse button
- Drag & Drop – press the *middle* mouse button over an item and while still pressing down drag it to the new location
- *Left* mouse button – sets the T0 cursor in waveform window
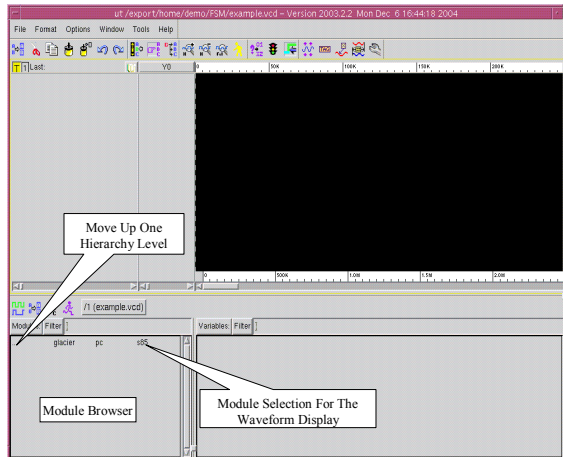
Veritools

Loading Files From the Menus

- File => Open /Close File
- Select File from the directory and click Open
- For high speed display of waveforms use "Create & Load Fast File"
- To create Fast Files offline:
- vdump -xn vcdfile newfile is vcdfile.fast (compression to ~100x)
- Or vdump -cxn vcdfile newfile is vcdfile.fast(compression to ~1000x)

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Module Hierarchy

Move Up One Hierarchy Level

Module Browser

Module Selection For The Waveform Display

- Modules in the file will appear in the Module Browser.
- Click on the module to go further down the hierarchy. A list of signals of the chosen module will be displayed
- To go up one hierarchy level click on ".."

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Viewing Signals

Signal Name Area

Select All
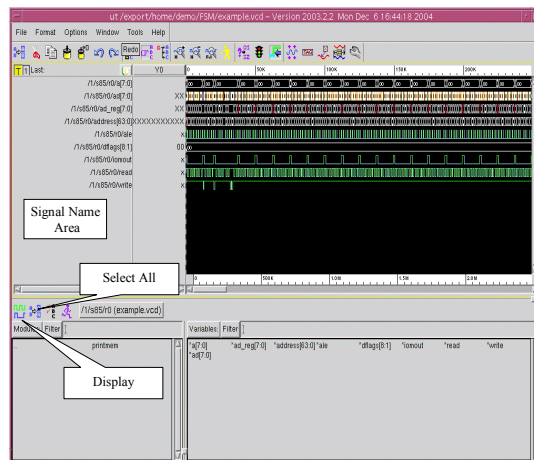
Display

- Select one or more signals
- Drag and Drop signals into the signal name area of waveform window
- Or press "Display" icon to add signals to waveform window
- Pressing "Display" icon with no signals selected toggles it into display mode, any signal selected will be added to the bottom of the display
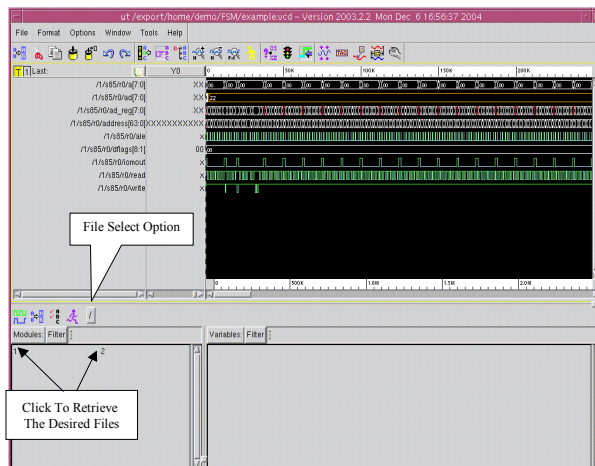- Use "Select All" icon to display all signals

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Working With Multiple Files
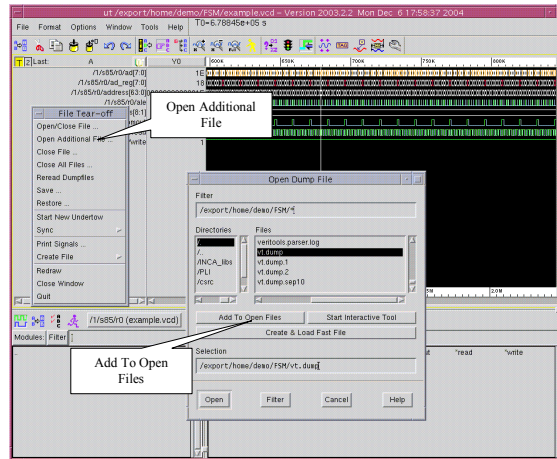
- To close the current file and open a new file press File => Open/Close

- To open an additional file along with currently loaded files press File => Open Additional File

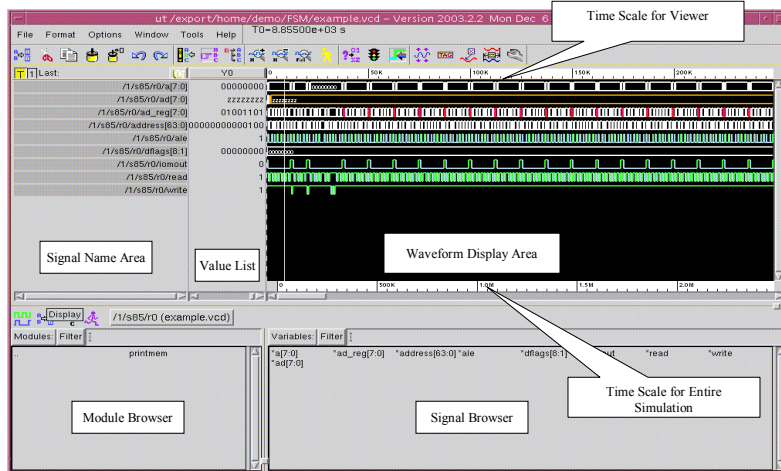- Or select the new file and click on "Add To Open Files"

Working With Multiple Files

- Numbers in the (e.g. 1 & 2) in the Module Brower window represent open files. Click on them to access modules of these files

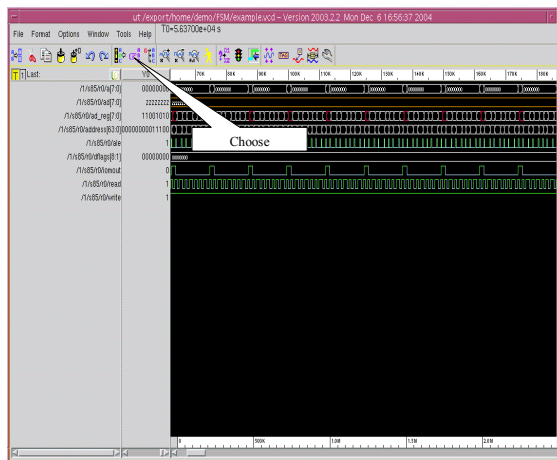- Or left click your mouse on "File Select Option" and select these files

Undertow Main Window

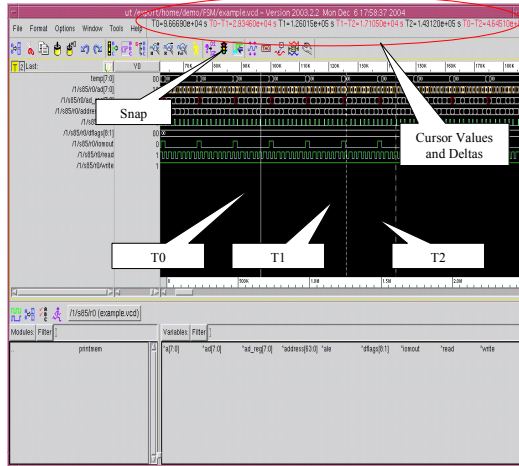# Choose

- Toggle to hide Module or Signal Browser

Setting Time Cursors

- Setting the Cursors T0, T1, T2
- T0 - *Left* click mouse button
- T1 - *Middle* click mouse button
- T2 – Shift + *Middle* click mouse button
- The time data along with the delta time data is displayed above icon bar
- If the "Snap" icon is toggled down, clicking the mouse button close to the edge of the signal will cause the cursor to snap to that signal edge (more reference for Snap in Configuration section)
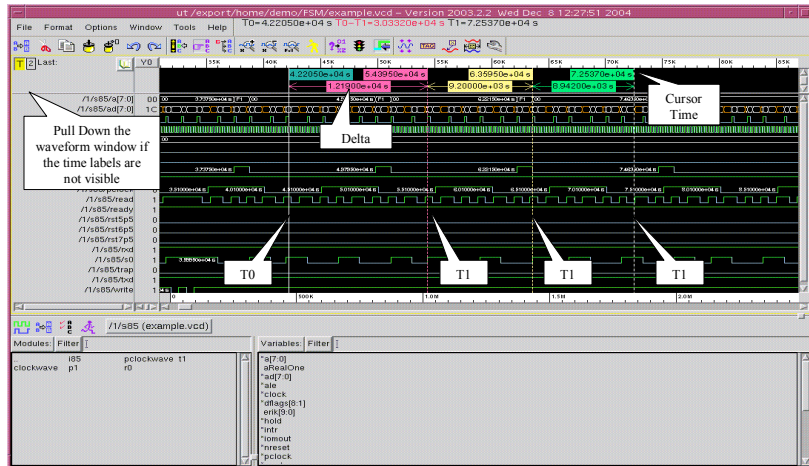
Multiple Cursors
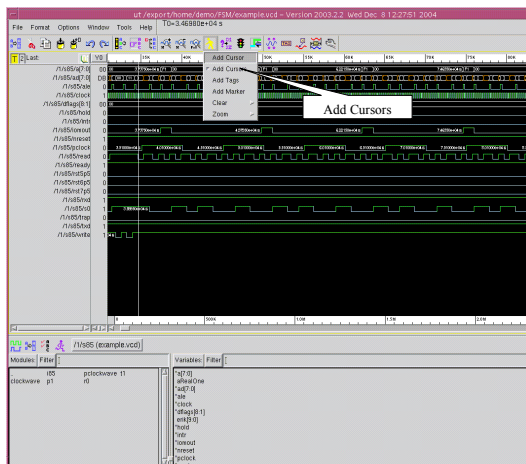
- Add multiple cursors to the waveform viewer
- Click on "Action" icon & select Add Cursors
- Click on left mouse button (T0) and then middle mouse button (T1) at the desired positions in the waveform window
- To add multiple cursors keep clicking middle mouse button (T1's)
- This will display cursor position time and delta time between T0 and T1's
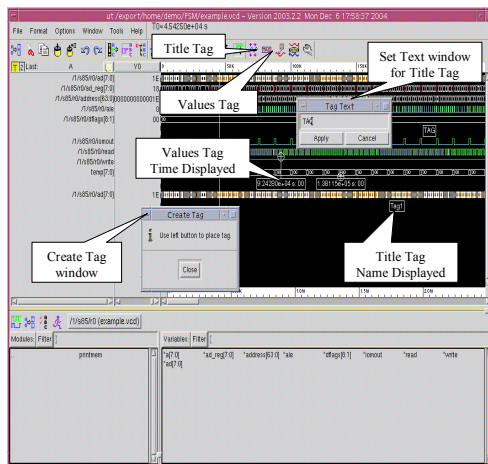
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Multiple Cursors

Placing Tags

- Tags mark Title/Values/Measure(delta) on the waveform window
- To set Title tag click on Window => Tags -> Title or click on "Title Tag" icon
- Click on the *left* mouse button on the waveform window to set the tag at the desired location
- To set the text on the Title Tag right click on it and select "Set Tag Text" Tag Text window will appear
- To set Value Tag click on Window => Tags -> Values or click on "Values Tag" icon and click *left* mouse button on the waveform window
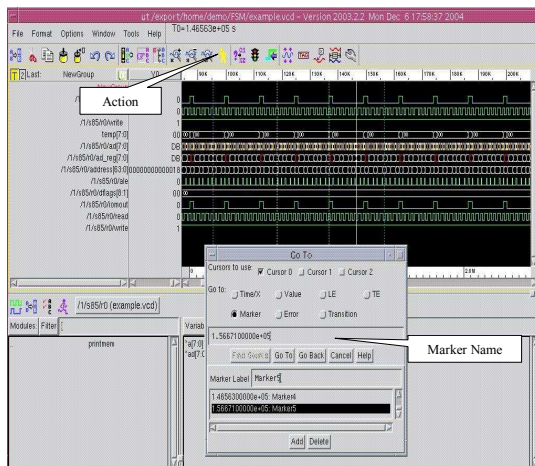
Placing Measure Tag
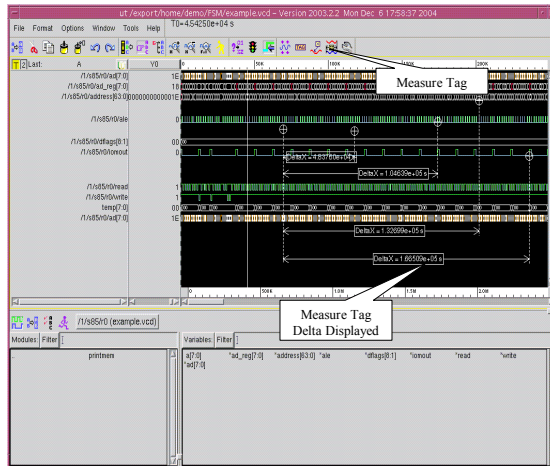
- Measure Tag helps draw timing diagrams fast
- To set Measure Tag click on Window => Tags -> Measure Tag or click on "Measure Tag" icon
- Click *left* mouse button to set first Tag and then click *middle* mouse button to set subsequent Measure Tags
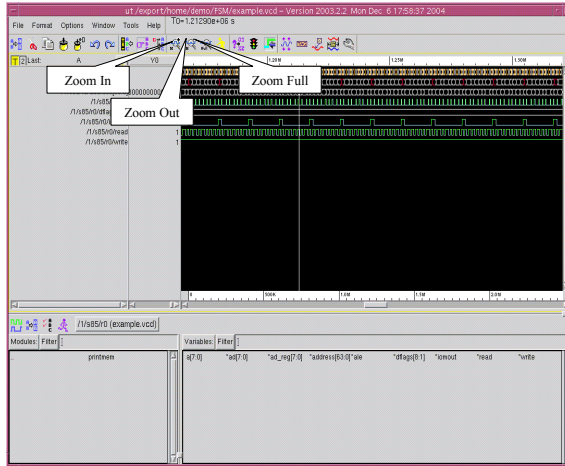
Placing Markers

- Action => Marker
- Marks the time with a user given name
- Click on waveform window to select the marker location
- Window will pop up with option for marker name
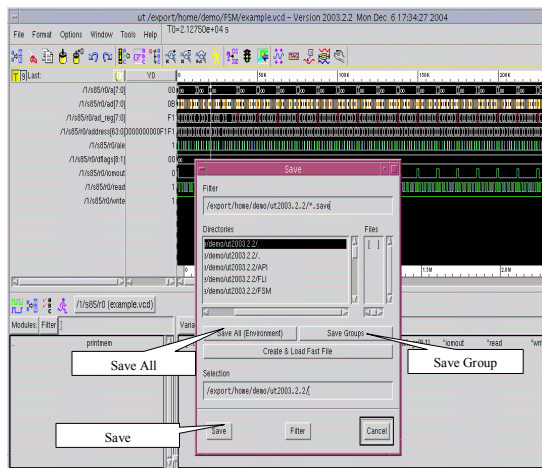- Enter the marker label and click Add to add this marker

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Zooming Waveform Window

- Zoom: click *left, left,* & *right* mouse buttons on the bottom time bar
- Or click *right* mouse button and slide the mouse
- Or use "Zoom In", "Zoom Out" & "Zoom Full" icons

Save Session

- File => Save
- Save - Saves the names of the signals currently displayed
- Save Group - Saves the defined groups in the current session
- Save All - Saves the setting of the current display: signals, cursors, markers, groups, etc.

Restore

- File => Restore, restores previously- saved files
- If the file contains a list of signals, Undertow displays those signals, but only if the signals exist in the current model
- If the file holds grouped definitions, Restore adds those groups to the current set of groups
- If you used the Save All (Environment) option to create the file, then the viewing environment is restored
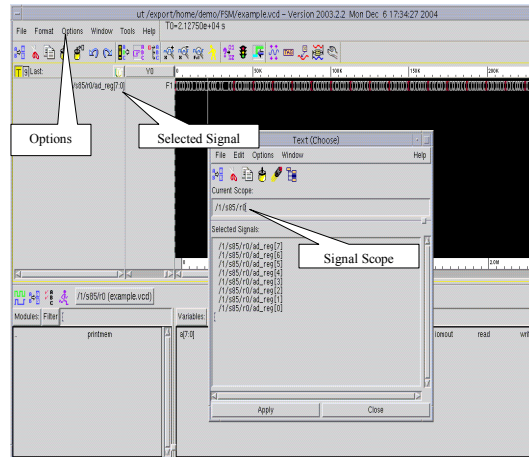
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Format Signal Values

Format

Digital Value
Representation
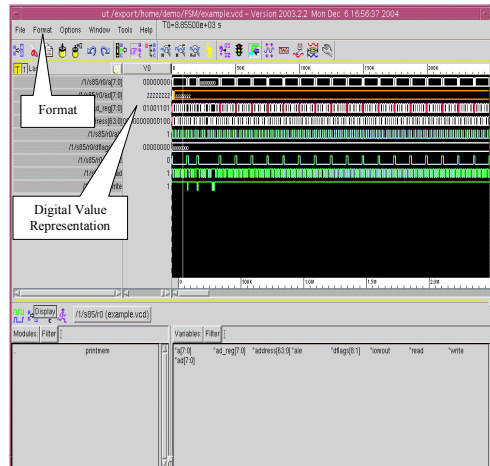
- Format => Hexadecimal/Binary etc.
- Format => Logic - Change the Analog Representation of a bus back to logic.
- Format => Analog - Creates Analog Representation of Digital Bus.
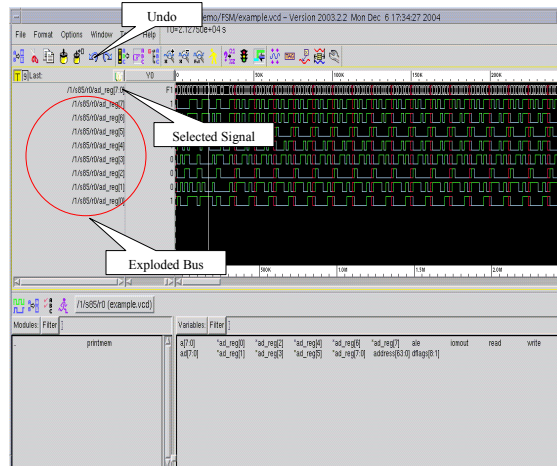
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Explode Bus

- Explode Bus expands every net of the given bus
- Options => Explode Bus
- New Explode Bus window will appear
- Drag and Drop Selected Bus in the Explode Bus Window
- Click Apply to add exploded bus back to display below selected signal
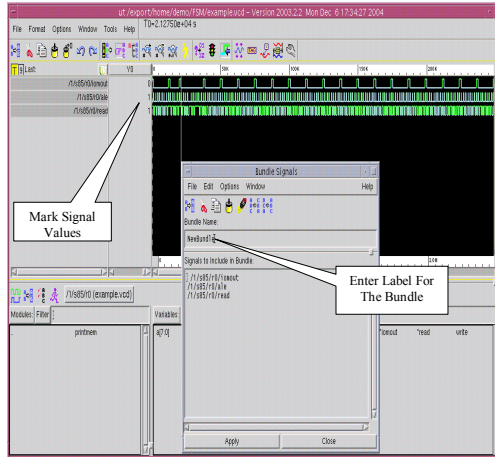
Veritools

Exploded Bus

- Use Undo to remove the exploded bus signals
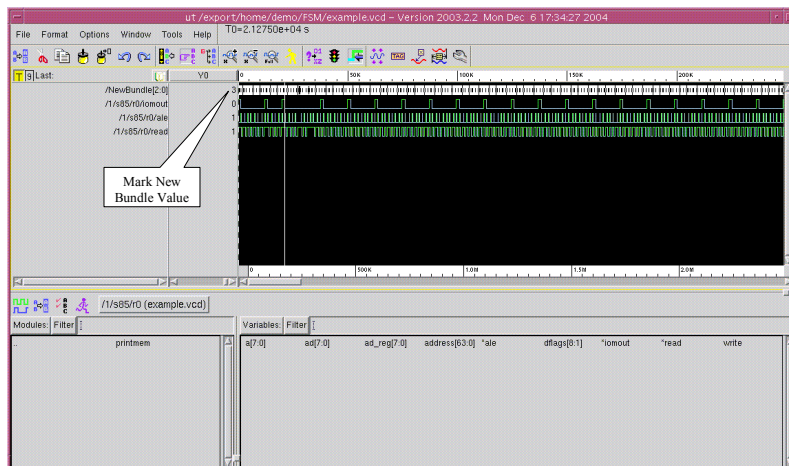
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Bundle Signals

- Bundle allows different signals to be packed together and display their joint value
- Options => Bundle Signals -> New
- New Bundle Signals window will appear
- Select the Signals
- Drag and Drop these signals into the Bundle Signal area
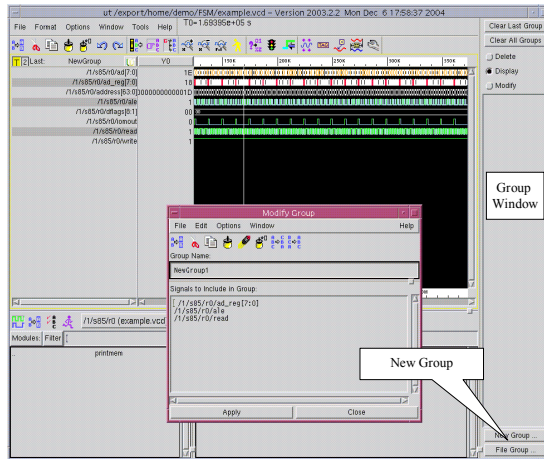- Provide a new label for the bundled signals
- Click Apply

Bundle Signals

Making Groups
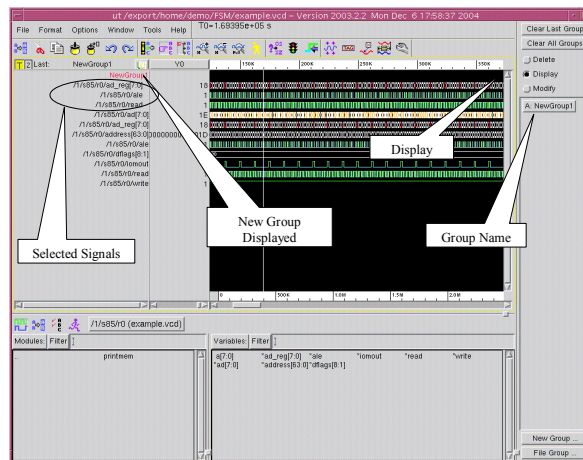
- Groups – Displays selected signals together
- Select "Groups" icon and in the Group Window click on New Group.
- Modify Group window will be displayed
- Drag & Drop selected signals into the window
- Provide a group name
- Apply

Displaying Groups

- Display - Click on the Display button and click on your group
- The group name will appear in red font at the top of the Signal Name Area
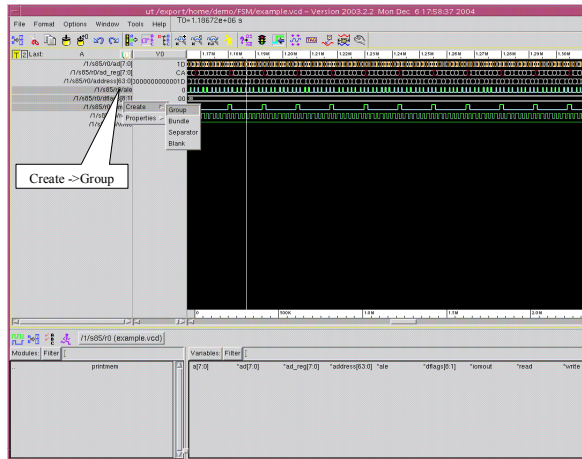
Groups

- Or to add a new Group select signals & *right* click your mouse button and select Create->Group option
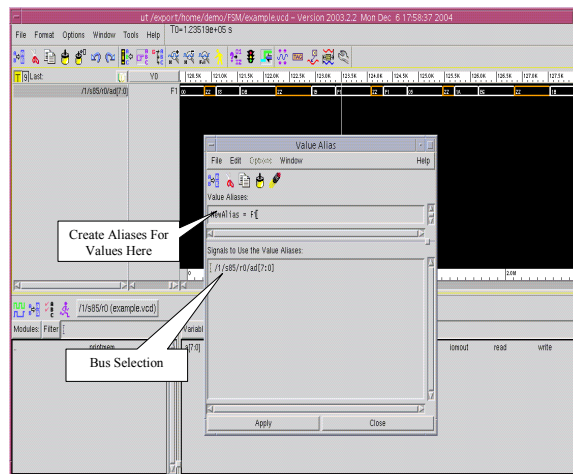
Alias, Value

- Alias, Value will provide a name label to the signal values
- Options => Alias, Value
- A new Value Alias window will be displayed
- Drag & Drop signals or have signals selected for alias to apply on them

Alias, Value
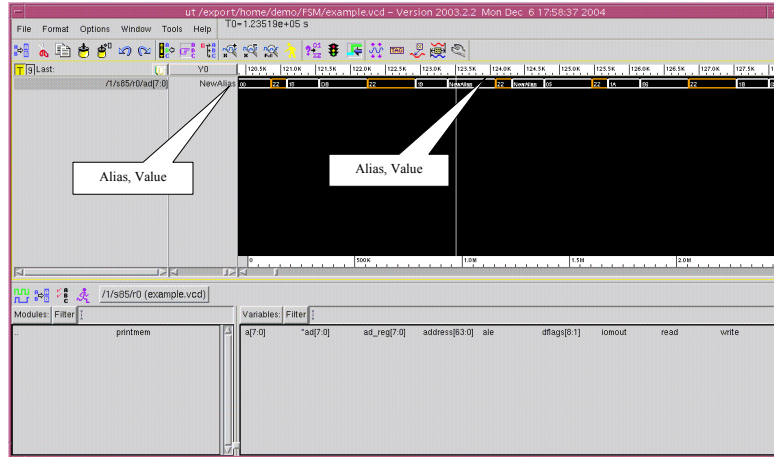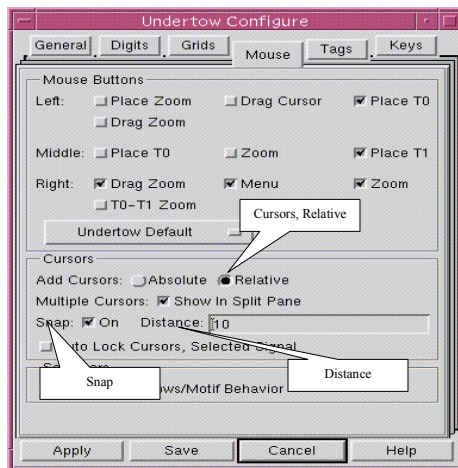
Configuration

- Configuration window allows the user to make configuration settings for the UT
- Window => Configuration
- Mark settings of cursors in the Mouse Tab.
- Adjust the values of "Distance" in Snap option based on signal frequency
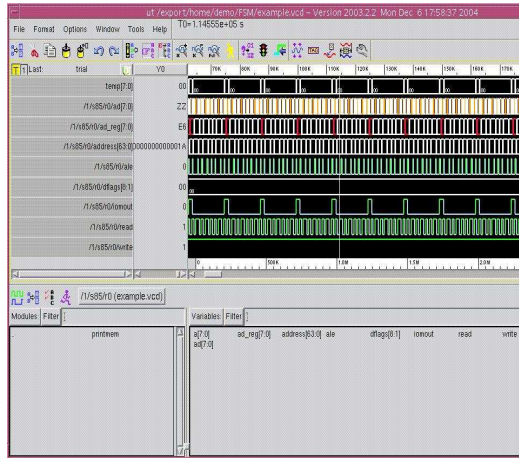
Fit To Pane

- Window => Fit To Pane
- Select Signals
- Enlarges Vertical size of the selected signals, to fit the pane of the viewer
- Or use the Fit To Pane icon

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Adding Additional Panes
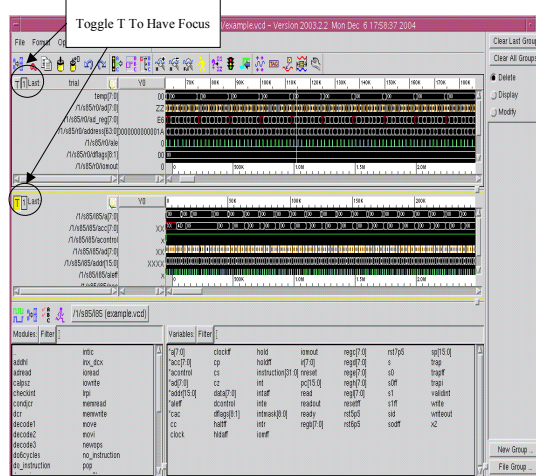
- Window => Panes ->Add New Pane, Time. Adds a new Pane, using the same time axis
- Add New Pane, Arbitrary X – Adds a new pane with an undefined x axis. Use this option if the horizontal scale is not single precision time or any other variable, frequency, voltage, current etc.

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Go To
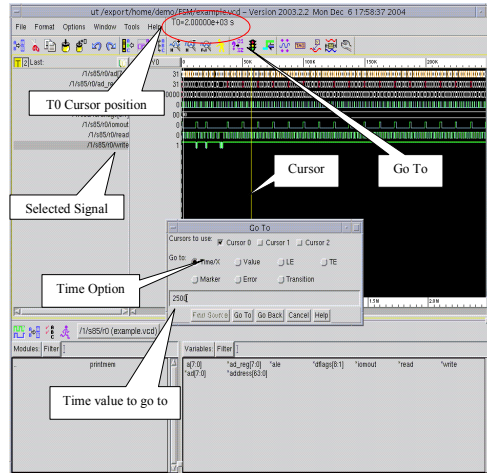
- Go To – Jumps the cursor to the desired Time/Marker/Value/Trailing Edge(TE)/ Leading Edge(LE) position
- Select the signal for Go To operation
- Select Go To icon
- Click on the "Time/X" button in the Go To window
- Select time or value on signal to go to

Labels in image: T0 Cursor position, Selected Signal, Time Option, Time value to go to, Cursor, Go To

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Go To – Time/X

Label in image: Mark The Cursor Position (T0)

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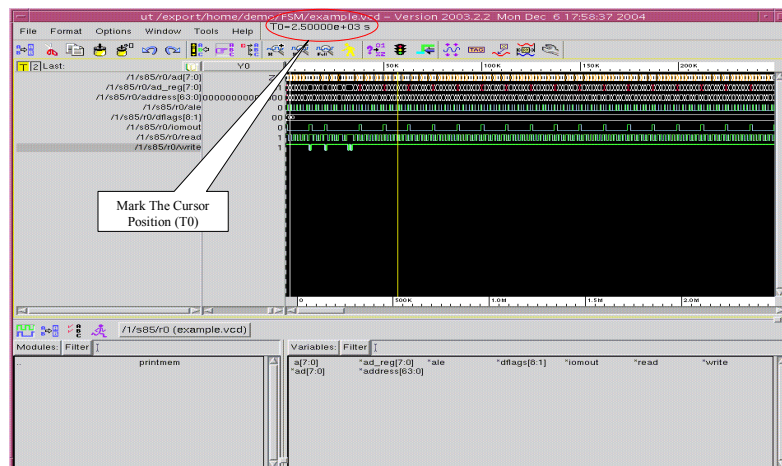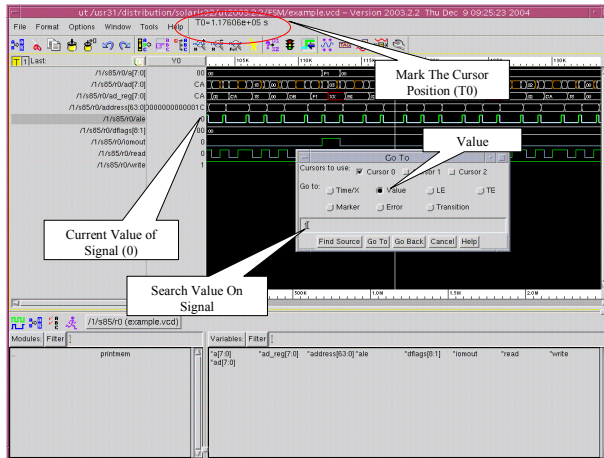
Go To - Value

- Select the signal for Go To operation
- Select Go To icon
- Click on the "Value" button in the Go To window
- Select Value on signal to go to.
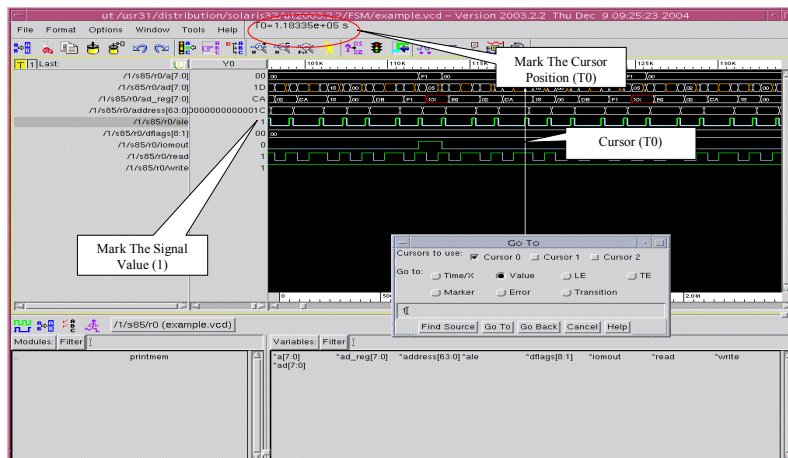
Go To - Value

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End of Undertow Basic Features tutorial …

Go back to the Main Menu

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Undertow
Analog Features

Veritools

Fast file and load input
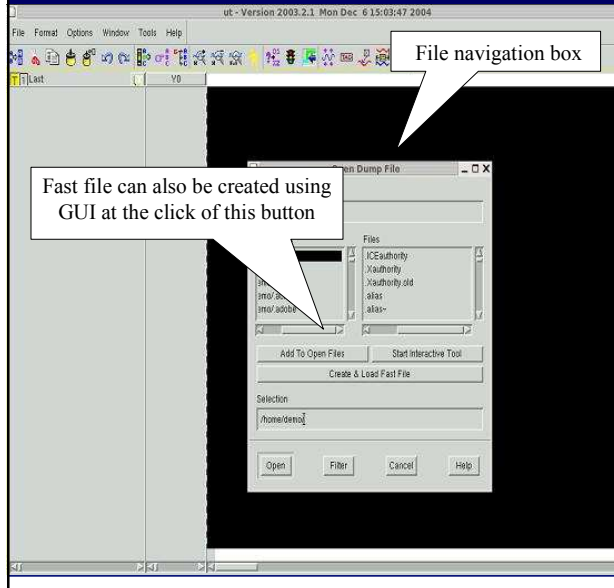
- Fast file can be created using an option
- Load input file using navigator button

Add signals
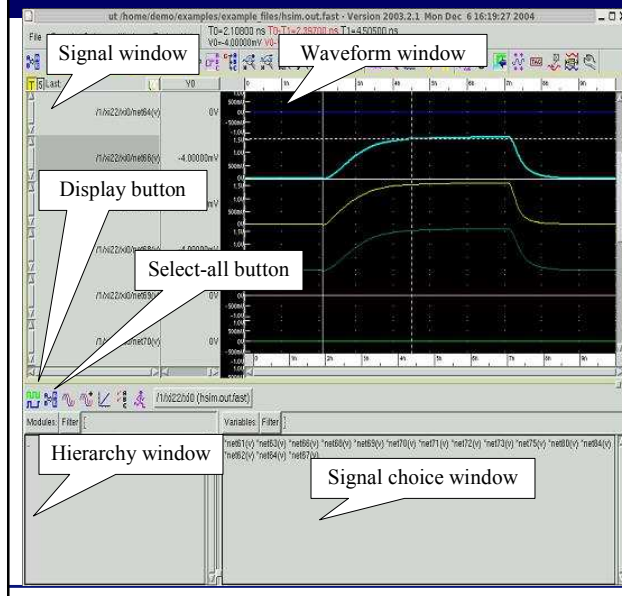
- Click on hierarchical module to list signals of the module
- Highlight the signals and click 'Display' button
- 'Select all signals ' option available
- Moving mouse over any button highlights its function

Group signals

Group button

Grouping box

- To group, display, modify and delete signals collectively
- Group of signals can be named collectively

Overlay signals

Overlay buttons

Overlaid waveform

Two waveforms

- Overlay option to superimpose signals
- Tools=>Analog Analyzer =>Overlay waveforms
- Drag and drop signals into the pop-up window
- Click Add to overlay the waveforms

Cursors & Measurement
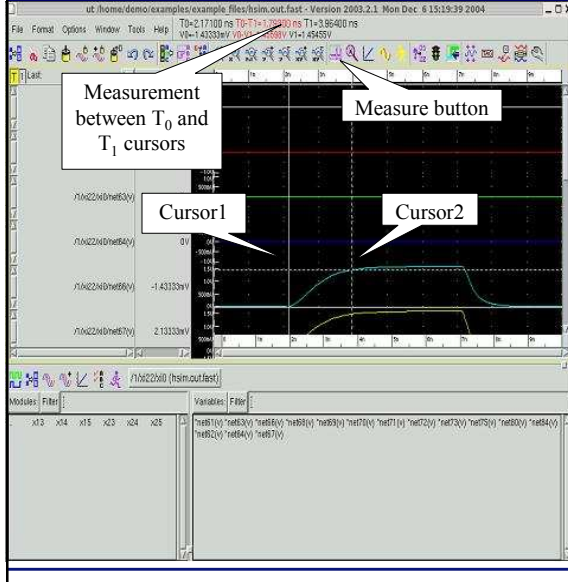
- Three cursor (T_0, T_1, T_2) measurement available
- T_0: Left click of mouse
- T_1: Middle click of mouse
- T_2: Shift key + Middle click of mouse

Measurement between T_0 and T_1 cursors

Measure button

Cursor1

Cursor2

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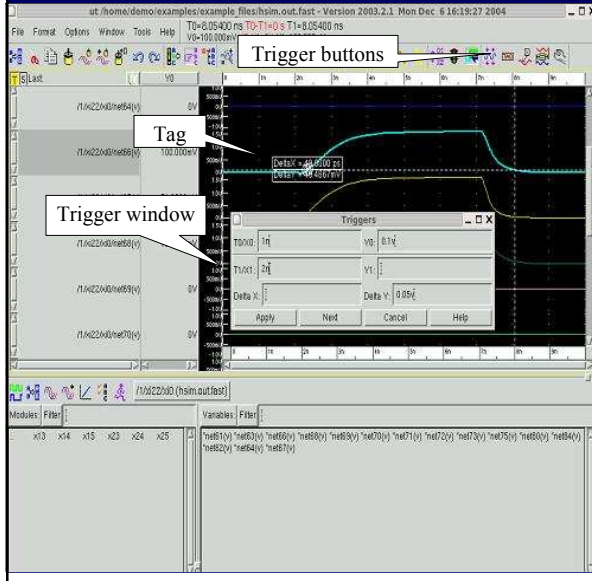
Tags & Trigger

- Option to create tags
- Title tag, Value tag, Measurement tag
- Trigger option identifies and drops tags at user specified events

Trigger buttons

Tag

Trigger window

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Goto option
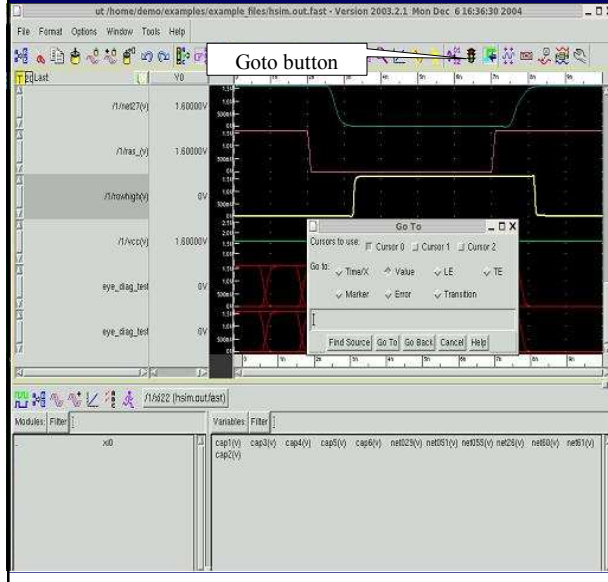
- To reach a point in x-axis or y-axis by virtue of its value, or time or transition type
- Likewise for each cursor

Goto button

Analog-Digital conversion

Equivalent digital pulse

Threshold points
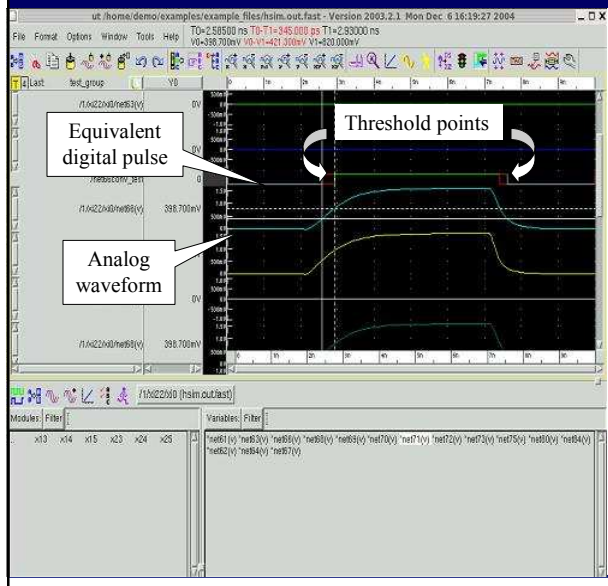
Analog waveform

- To convert an analog waveform into its equivalent digital pulse
- User-defined threshold voltage, rise and fall times
- Usage: Tools=>Analog analyzer=>Convert to digital
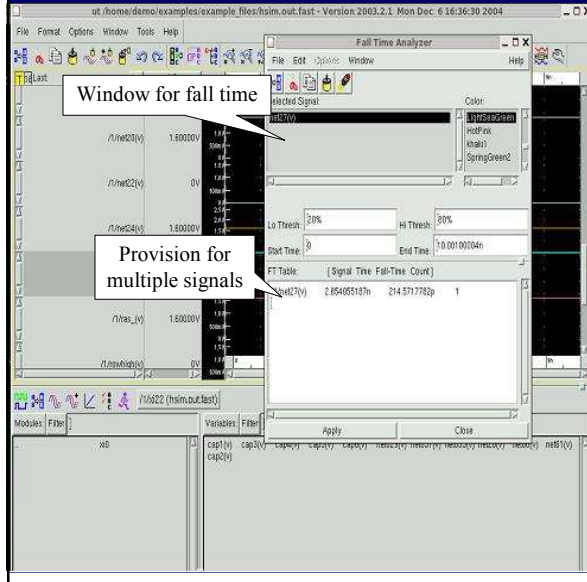
Rise and fall times

- To measure rise and fall times between user-defined thresholds
- Ability to focus on bounded start and end times instead of full waveform
- Usage: Tools=>Analog analyzer=>Fall time
- Drag and drop signals into the fall-time analyzer window
- Likewise for rise time

Window for fall time

Provision for multiple signals

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Pulse width analyzer
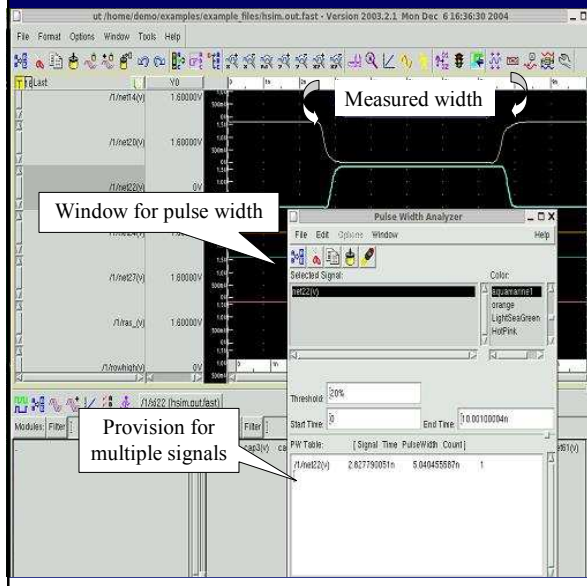
- Can measure width of signals
- Ability to measure for multiple signals simultaneously
- Usage: Tools=>Analog analyzer=>Pulse width analyzer
- Now drag and drop signals

Measured width

Window for pulse width

Provision for multiple signals

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Eye diagram analyzer
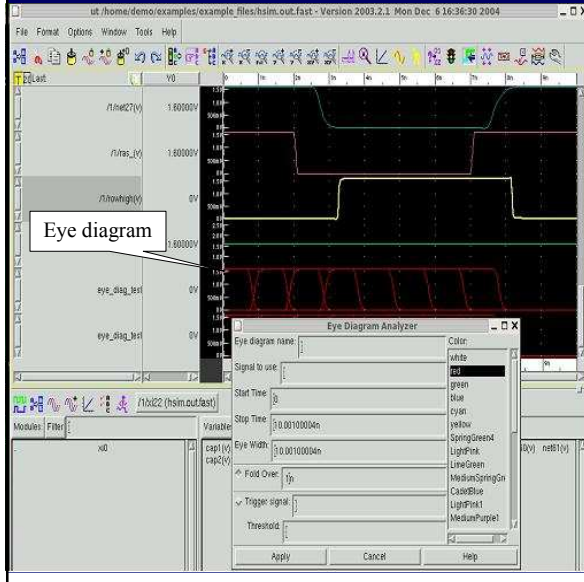
Eye diagram

- Fold over Eye diagram of signals can be generated
- Provision to vary eye-width
- Provision to focus on desired time points of signal and generate eye diagram for it
- Usage:Tools=>Analog analyzer=>Eye diagram analyzer

Special functions

Mathematical functions

Analog expression window
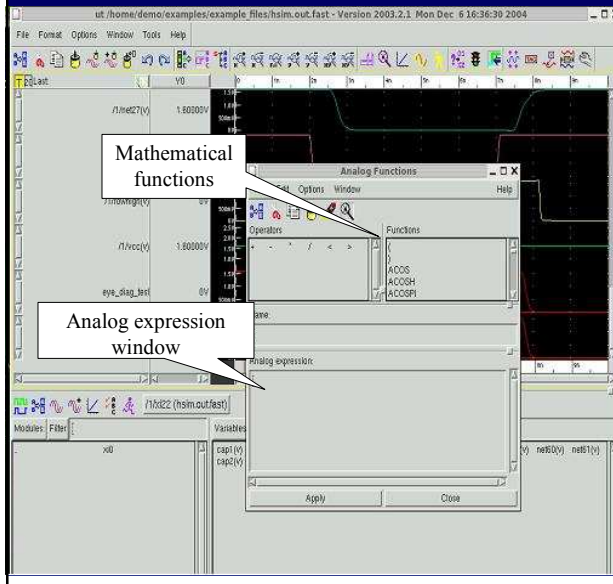
- Provision to create analog expressions, mathematical functions, trigonometric functions
- Feature to create filters
- Usage: Tools=>Analog analyzer=>Special functions

- End of Undertow Basic Features tutorial …

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Undertow Suite

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Set the license environment variables

Set up environment variable for the license manager:
- setenv UT_ROOT_DIR path/undertow (distribution directory)
- Set up environment variable for the Undertow root directory:
- setenv VERITOOLS_LICENSE_FILE path/directory (holding the license file)

For more details on setting up the flexlm license manager,
see Appendix A

Veritools

Start Undertow Suite in batch mode

- Replace the word "verilog" on your command line with "ut –iv" for batch operation of the Undertow Suite, and add in a command to identify your signal file name

  -sigfile *waveform_file_name*

  verilog –f *design file command-line-args*

  becomes

  ut –iv –f *design file command-line-args* –sigfile *abc.sigs*

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Start Undertow Suite in interactive mode

- Place ut –iv –xl in front of the word "verilog" for interactive operation, and add a command to identify your signal file name

  -sigfile *waveform_file_name*

    verilog –f *design file command-line-args*
              becomes

  ut –iv –xl verilog –f *design-file command-line-args* –sigfile *abc.sigs*

Veritools

Source code & waveform windows

Hierarchy Browser

Source Code Browser

Source Code Window

Signal Selector

Waveform window
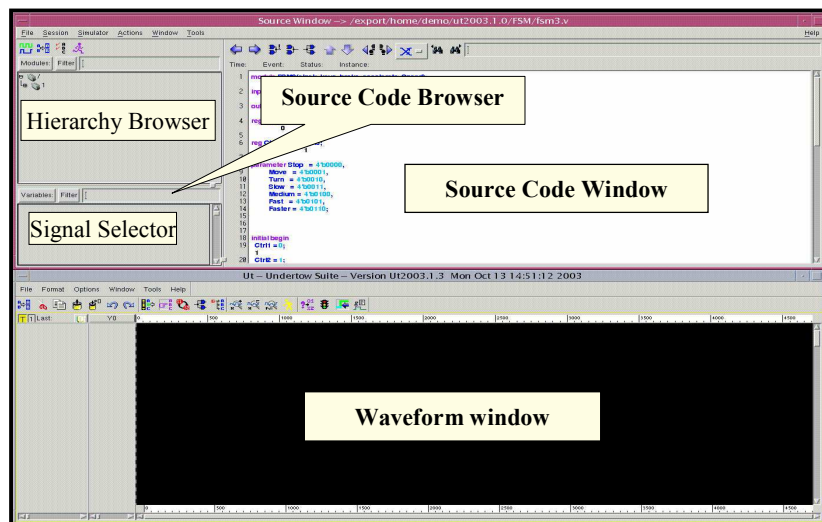
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Open the design hierarchy
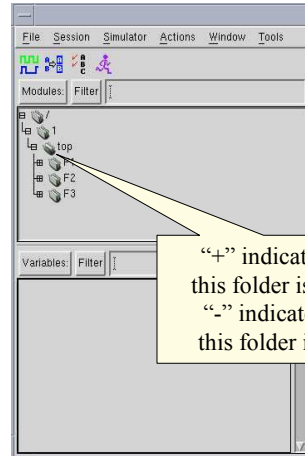
- Press the left mouse button on the "+" sign to open down one level. The "+" will change to a "-"
- Press the "-" sign to close all levels below this level

"+" indicates that this folder is closed
"-" indicates that this folder is open

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Display the source code for any module
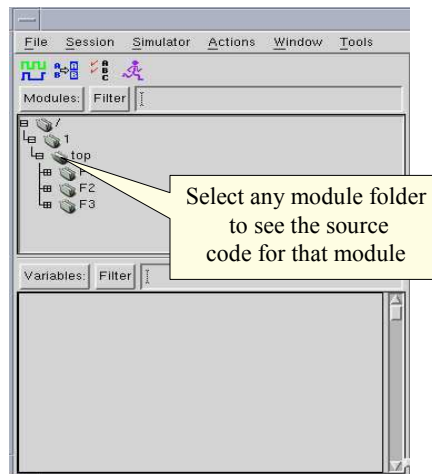
- Select the folder for a Module to display the source code for that module in the Source Code window.
- The folder for the code displayed in the source code window will be indicated by an open folder icon.

Select any module folder to see the source code for that module

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Select a module & display signals names
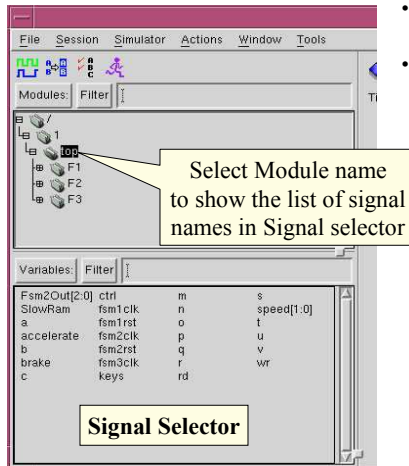
- Select the module name in order to see the signals listed in the Signal Selector
- The module name will be reverse highlighted to indicate which module has signals displayed in the Signal Selector

Select Module name to show the list of signal names in Signal selector

Signal Selector

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Select signals & display waveforms

Use left mouse button to select signals to be added to waveform display
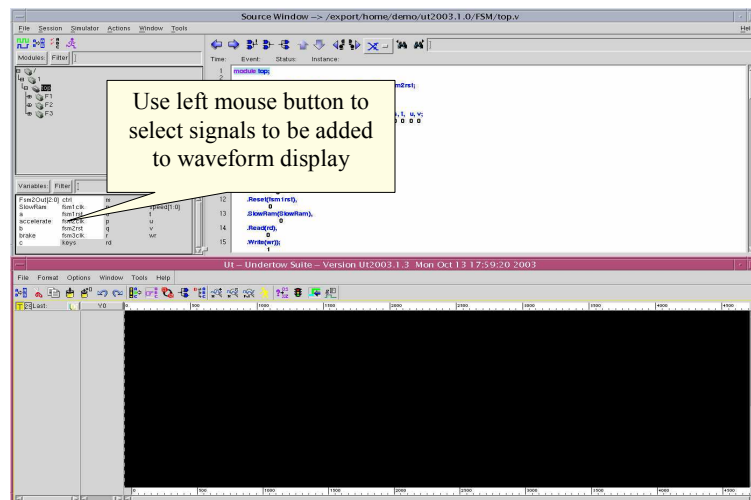
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Use drag & drop to display signals

Use the middle mouse button drag and drop to drag the selected signals to waveform display signal name area

Select signals using the "Display" icon

- Or you can press down the Display icon and then select the signals you want displayed in the waveform window
- Drag the select over many signals to select more than one signal at a time

Use "All" to select all signals at a level
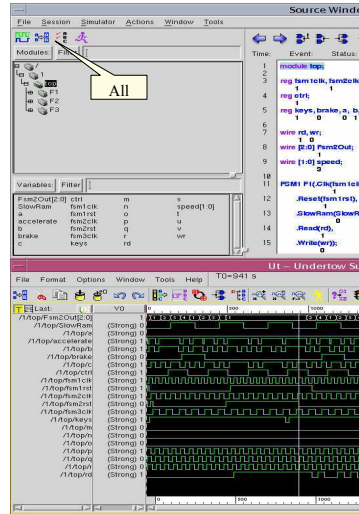
- Once the Display icon is toggled down, users can press the "All", icon to select all signals at this level, to be added to waveform display.
- Note, Undertow is extremely fast, even if this had been a 2 gigabyte waveform file, the signal data would have been displayed on Undertow almost instantly, provided the data is either in an optimized file or a fast file format.

Use "Snap"

Values are shown under the signal name

Time for T0 cursor shown here

Set Snap icon toggle down to enable snap

Snap T0 cursor to edge of signal
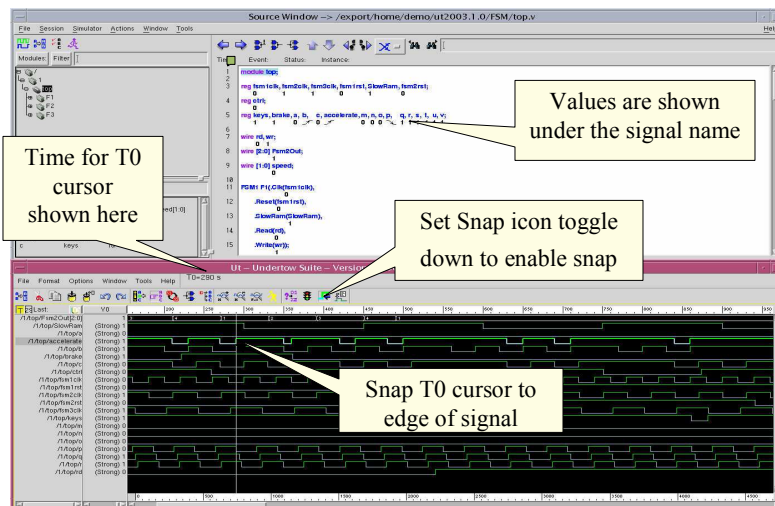
Use "Snap to Source"

Finally, when you snap to the signal edge, the line of source code that caused this transition will be highlighted in blue

First toggle down the "Snap to Source" icon

Second, snap to edge of signal where you want to see the source code that caused this transition

Veritools

Trace drivers on source code window

- After snapping on an edge on the accelerate signal , the assignment for accelerate is displayed;

    accelerate = a|b|c

  "accelerate" is going from one to zero, the signal "b" is also going from one to zero.

  To trace back the driver for "b" toggle the "Show Driver" icon down.

  Then select "b", by pressing the left mouse button on "b".

Veritools

Find the correct assignment for "b"

Press the "Down" icon to see other assignments for "b".

Notice that the assignment that is shown indicates that a "0" is being assigned to "b", but that the value of "b" at the current simulation time is shown to be going from a "zero" to a "one"

All of the assignments for "b" will be shown in the detail window at the bottom of the Source Code window

Detail Window

Find the right assignment for "b"

Looking at the signals values, to determine if this is the correct assignment for "b".

Finally, next select "r" to next trace back the assignment for "r".

Find the correct assignment for "r"

Use the "UP" and "Down" icons to find the correct assignment for "r", by examining the signals values and the values being assigned to the variable "r" for each assignment.

The assignments for "r" are shown in the detail window.

Open Schematic and State Windows
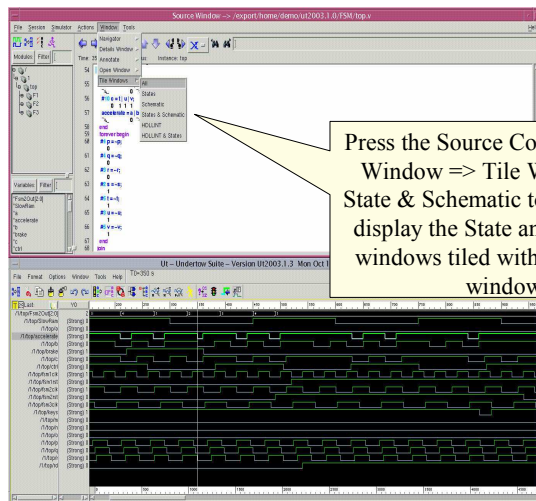
Press the Source Code menu item Window => Tile Windows => State & Schematic to bring in and display the State and Schematic windows tiled with the existing windows

Schematic & State windows

State Diagram Window

Schematic Window
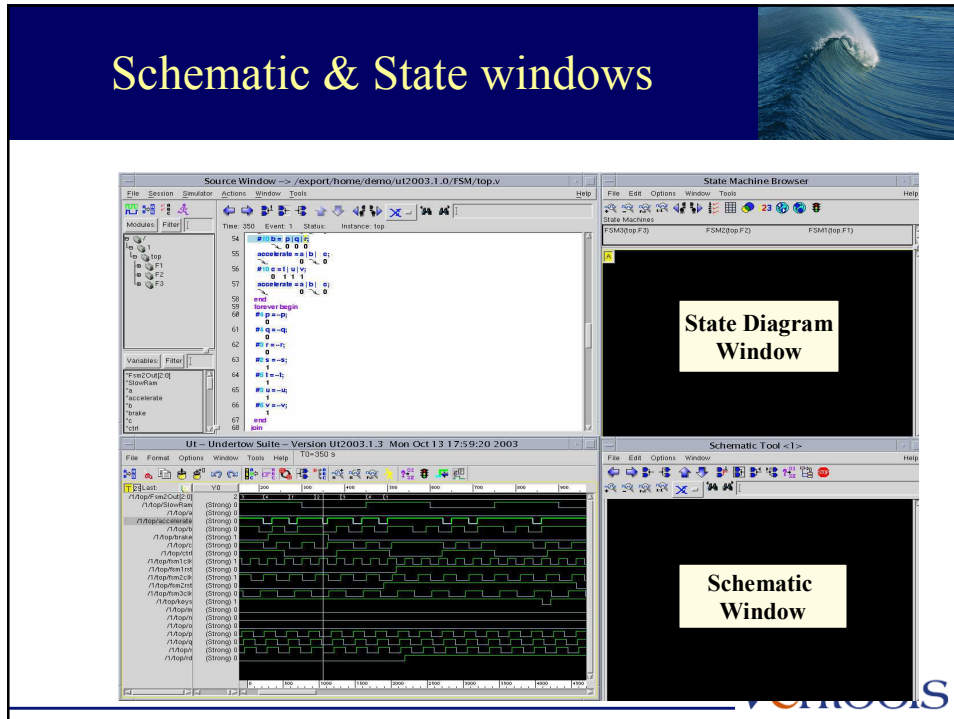
Display the schematic for a module

Drag and drop the module "top" from the hierarchy browser to the schematic window, or right click on the module name

To descend down into this block, double click on the black space inside of this block.
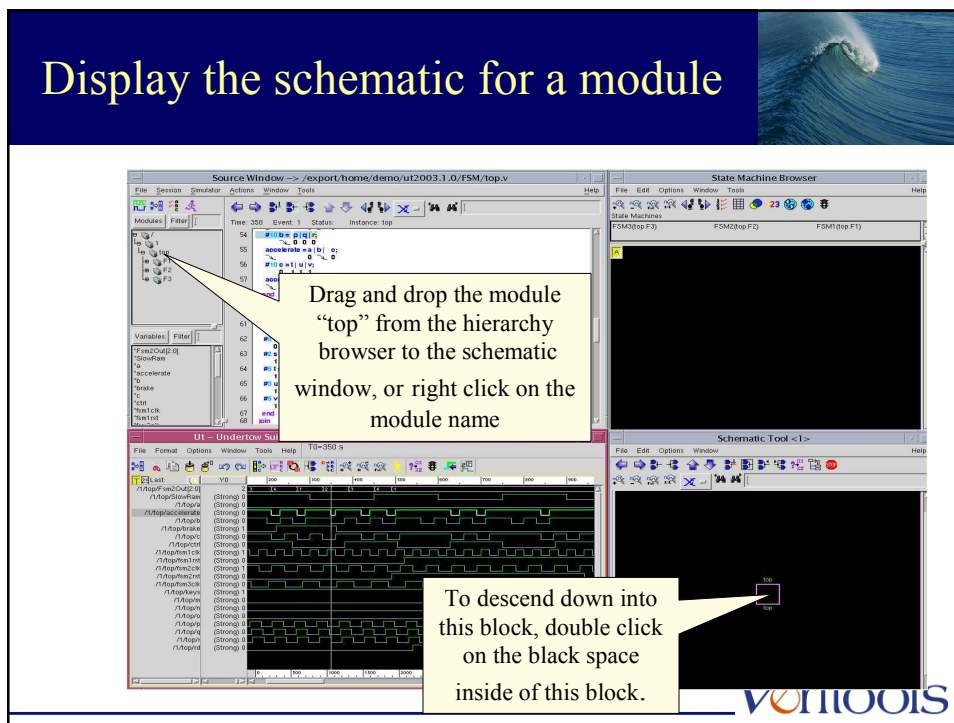
Use "Show Whole Schematic"
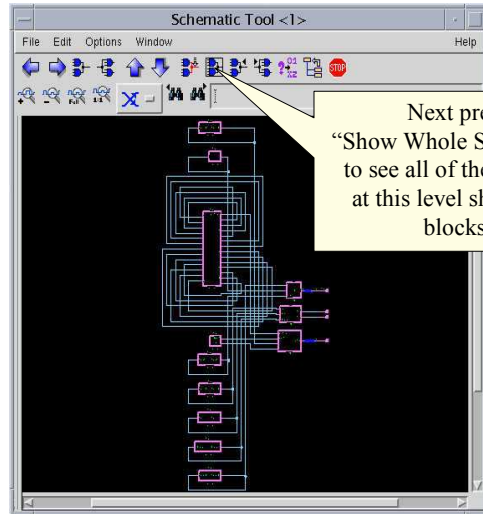
Next press "Show Whole Schematic" to see all of the modules at this level shown as blocks.

This will show you the modules and blocks located one level down from "top".

Use "Show Whole Schematic"
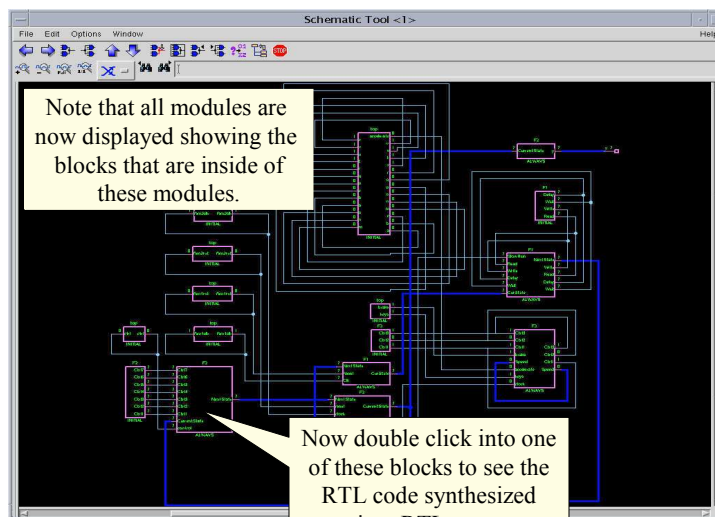
Note that all modules are now displayed showing the blocks that are inside of these modules.

Now double click into one of these blocks to see the RTL code synthesized into RTL gates

Display the synthesized RTL block

Press the "Update Values" icon to see the waveform values at the T0 cursor annotated onto the schematic pins

Double clicking in black space in the block shows all elements inside this block

Selecting any pin first and then double clicking limits the schematic to only logic connected to this pin

Double clicking on any pin only displays the first level of logic connected to this pin
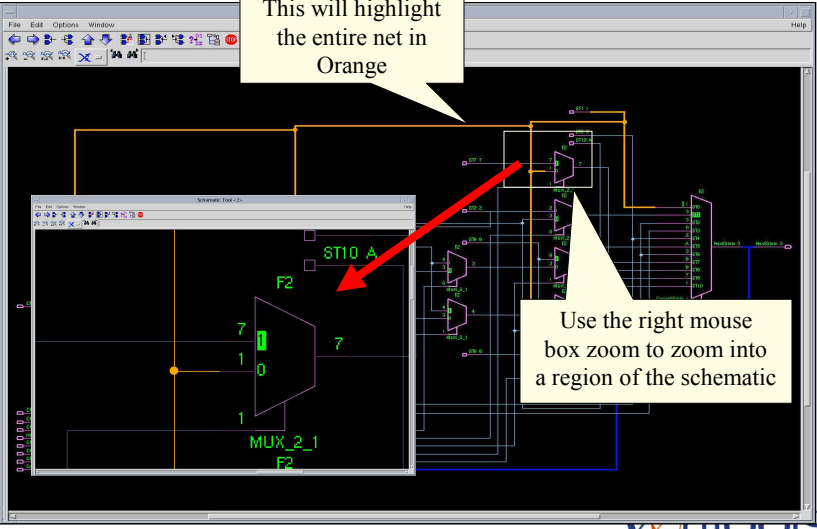
Detailed view of synthesized RTL Code

Select any net to be highlighted by first selecting the Highlight net icon

Then select a pin on that net

Use "Highlight Net"
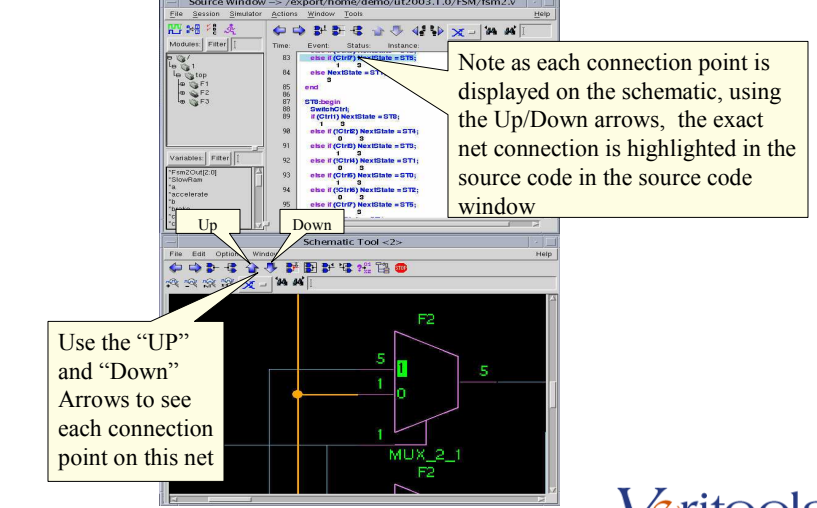
This will highlight the entire net in Orange

Use the right mouse box zoom to zoom into a region of the schematic

Schematic synchronized to source code

Note as each connection point is displayed on the schematic, using the Up/Down arrows, the exact net connection is highlighted in the source code in the source code window

Use the "UP" and "Down" Arrows to see each connection point on this net

Select logic for "Back/Forward Tracing"
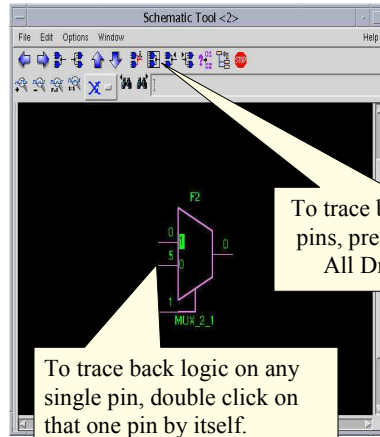
• Drag any element back to the same schematic window or to a new schematic window in order just to see just that element by itself

To trace back logic at all pins, press the "Expand All Drivers" icon.

To trace back logic on any single pin, double click on that one pin by itself.

Veritools

Trace back using "Expand All Drivers"
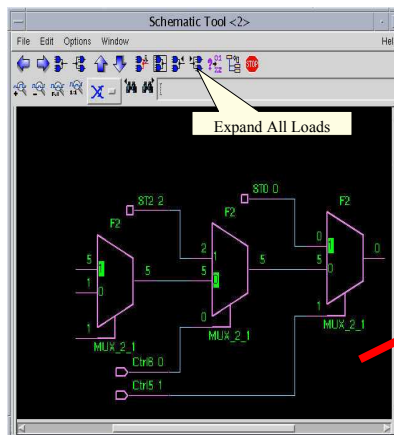
• To trace the logic forward to any level press the "Expand All Loads" icon to see the logic expand forward to any point in the design.

Expand All Loads
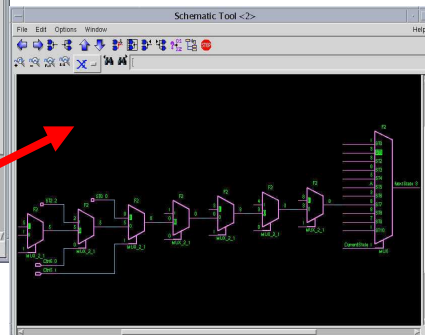
Veritools

Reorganize with "Tile All" windows

Select a state diagram from the State Diagram Selector

Use right Box Zoom to zoom into the desired area

Step a State Diagram

Step the state diagram forward or backward using the "Steps Forward" or "Steps Backward" icons

The double bubble indicates the current state

Display Multiple State Diagrams

Press Window => Add Pane Horizontal in order to add additional panes to the state diagram window
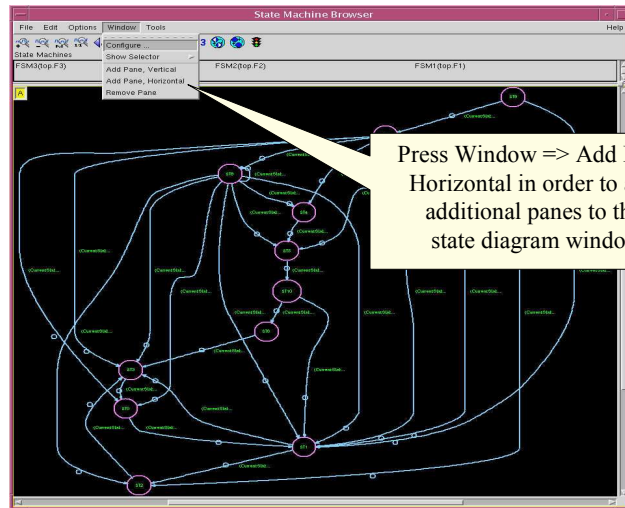
Set State Diagram to "A" for active

The yellow "A" indicates that this is the active state diagram, all icons will act only on the active state diagram

- Users can add and display as many state diagrams simultaneously as they require by adding in additional panes both in the horizontal or vertical direction and then selecting additional state diagrams
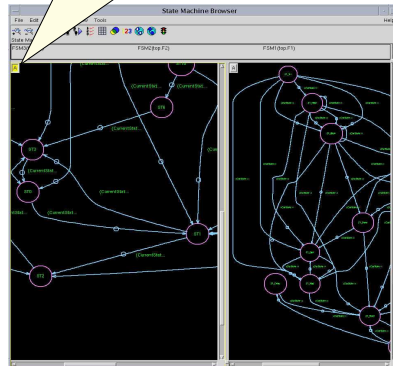
Find the assignment for any state on the source code window

Drag any state to the Source Code window to find where it is assigned

Find NextState on the Schematic

Drag NextState from the Source Code window to the Schematic window

The net for NextState will be highlighted in orange

State Variable on waveform window remains synchronized with State Diagram

The state in the state diagram window will be updated to synchronized with the state listed on the waveform

Pressing the GoTo button will cause the T0 cursor to go to the next transition point on the highlighted state variable "CurrentState"

Appendix A: License Installation

Veritools license requires the flexlm/lmgrd server. If you do not have it, you can download it (and the "verid" deamon) from our website for your corresponding platform at: http://www.veritools.com/download_latest.shtml

- Contact support@veritools.com for username & password.
- %gunzip LicenseMgr_****.tar.gz %tar xvf LicenseMgr_****.tar
- The following will be generated: LicenseMgr/ LicenseMgr/install_license.txt LicenseMgr/license_support.txt LicenseMgr/lmgrd LicenseMgr/lmutil LicenseMgr/verid
- Follow the instructions in the install_license.txt & license_support.txt files for installing the License Manager and the "verid" daemon.
- 1. Append your Veritools license code into your license file or save it as 'license.dat' in the LicenseMgr directory.
- 2. Use the following UNIX command to set the permissions for your license file. For example: %chmod 444 license.dat
- 3. In your shell start up script (~/.cshrc), set the LM_LICENSE_FILE environment variable to point to your license file. setenv LM_LICENSE_FILE <path>/license.dat
- 4. Use the foll. UNIX command to source your .cshrc file %source ~/.cshrc II) Make sure that your hostname in your license corresponds to your machine. %hostname should give you your hostname. Make sure the license.dat file has the correct hostname. If not, modify it. (CONTINUED)

Appendix A: License Installation cont.

Stop and restart your license server from your LicenseMgr directory.

- %./lmutil lmdown -c license.dat //to stop
- %./lmgrd -c license.dat -l log.txt //to start
- %./lmutil lmreread -c license.dat can be used if the lmgrd is started in the first place.
- If you modify the license.dat file, you should reinitialize lmgrd by running lmreread.
- %./lmutil lmstat -c license.dat //will let you know whether the license is up or not.

If you have any problem with getting your license up, you can try the following:

- 1. Set the hostname of your machine to be its ip address.
- 2. Replace hostname in the license file with its ip adress.
- 3. Change the VENDOR line in the license file to DAEMON /path/verid

Veritools

Appendix A: License Installation cont.

Also, once your license is up and running, make sure you set the following environment variables and source your .cshrc file:

1. setenv UT_ROOT_DIR <path_to_undertow_installation_directory> UT_ROOT_DIR points to the installation directory of the Undertow Suite.
2. setenv UT_WORK_DIR <path_to_working_directory> Sets the default directory for Undertow Suite file dialogs. You can set it to the current directory.
3. PATH variable: If the Undertow executable (ut) is in a directory path that you specified in the UNIX PATH variable, then you can specify only the executable name (ut) when you start the software.
4. setenv LM_LICENSE_FILE <path to license file>/license.dat Set the LM_LICENSE_FILE environment variable to point to your license file.
5. Then source your .cshrc file before you use ut: %source ~/.cshrc
6. Verify the above as follows: %echo $UT_ROOT_DIR %which ut These should give you the path to the Undertow installation directory

Veritools

Linking in the Veritools' PLI

- To link in our PLI and use Undertow with various simulators, please refer to:
  http://www.veritools.com/literature/FSM_README.html
- This will give you step-by-step instructions for simulating the Verilog design (FSM example) using various simulators like FINSIM, VSIM, VCSI, NCSIM, NC Verilog XL, NC Verilog and Verilog XL. Also included are instructions for linking the PLI and examples for using Undertow in interactive mode with these simulators as well as batch mode.
- Please refer to the /FSM directory for the FSM example design. Other README's are also available.

Veritools

- End of Undertow Suite tutorial …

Go back to the Main Menu

Veritools

Veritools

Using Simulators VCS, Modeltech, NCSIM With Undertow Suite

STEPS FOR VCS

- Source environment variables

    For example, envsource has all the environment variables set up.

    You can change the paths accordingly.

    ------------envsource file contents-------------------------------

    setenv VCSI_HOME <path where VCSI is installed>

    setenv DEFAULT_VCS_HOME <path where VCSI is installed>

    setenv VCS_HOME <path where VCSI is installed>

    setenv TMPDIR /tmp

    setenv VCS_NETHOST vt1

    setenv VCS_LTD_LICENSE 1

    setenv VCS_CC cc

- vtplivcs.o and vt_vcs.tab are present in our PLI directory

VCS contd.

- \<source\> is the file that contains the source code files for Simulation
- To make the source file: add iv.v (found in our distribution directory) at the top with top level file next followed by all the .v files needed in simulation.
- Contents of iv.v file

```
// iv.v
module vtInteractive;
initial
        $vtIv;
endmodule
```

Veritools

VCS cont.

- Add to source code close to top module

```
initial
begin
        $vtDumpvars();  /*dumps everything - created by our PLI routine.*/
        $vtTrace(1) /*enables event tracing of your complete design*/
end
```

- In the example(in our distribution directory), the above has been inserted in 'top.v' file.

Veritools

VCS cont.

- To compile through the simulator in interactive mode do as follows:

  vcsi <flags> -f source $UT_ROOT_DIR/PLI/vtplivcs.o –P
  $UT_ROOT_DIR/PLI/vt_vcs.tab

- For example,

  ./run_vcsi_int

  -------run_vcsi_int contents----------------------------------

  #!/bin/csh –f

  vcsi -Mupdate +vpi +cli +acc+2 -lm -line -f source

  $UT_ROOT_DIR/PLI/vtplivcs.o –P UT_ROOT_DIR/PLI/vt_vcs.tab

Veritools

VCS cont.

- To open the Undertow Suite in batch mode, the command lines is as follows:

  ut -iv -f <source> -sigfile <dump filename>

  <source> is the file that contains the source code files for simulation

  For example,

  ut -iv -f source -sigfile fsm.sigs -tracefile fsm.trace

  To view just the waveform,

  ut -v <signal_file>

  For example,

  ut -v vt.dump

- To open the Undertow Suite in interactive mode the command lines is as follows:

  ut -iv -vcs <vcs_simulator_executable> "<simulator_options>" -sigfile

  <signal_filename> -tracefile <trace_filename> -ivsimcmp "-f <file that lists

  all source code file names>"

  For example,

  ut -iv -vcs simv -sigfile fsm.sigs -tracefile fsm.trace -ivsimpcmp "-f source"

Veritools

STEPS FOR MODELTECH

- Sourcing environment Variables
   For example,
   ./envsource
   ------------envsource file contents----------------------------
   setenv PLIOBJS $UT_ROOT_DIR/PLI/vtpli_modtech.so
   setenv ModelTech <path where ModelTech has been installed>
- vtpli_modtech.so is available in our PLI directory.

Veritools

MODELTECH contd.

- <source> is the file that contains the source code files for Simulation
- To make the source file: add iv.v at the top with top level file next followed by all the .v files needed in simulation followed by "+libverbose" at the bottom.
- Contents of iv.v file
   // iv.v
   module vtInteractive;
   initial
          $vtIv;
   endmodule

Veritools

MODELTECH contd.

- Add to source code close to top module

  ```
  initial
  begin
      $vtDumpvars();  /*dumps everything - created by our PLI routine.*/
  end
  ```

- In the example(in our distribution directory), the above has been inserted in 'top.v' file.

MODELTECH contd.

- Compile through the simulator as follows:

  ```
  ./run_modeltech
  run_modeltech : script for running all modelsim commands.
  ---------run_modeltech contents--------------------------------
  #!/bin/csh -f
  if (-e work) then
          rm -r -f work
  endif
  if (! -e work) then
          vlib work #creates new design library work
  endif
  vlog -f source #compiles the verilog files into the work library
  #vsim -c -do 'run -all' top vtInteractive +VTCOMPRESS250 +VTVECTORVALUES
  ```

MODELTECH contd.

- To open the Undertow Suite in batch mode, the command lines are as follows:

  ut -iv -f <source_code_file> -sigfile <signal_file>

  <source_code_file> is the file that lists all the source code files.

  For example,

  ut -iv -f source -sigfile fsm.sigs

  To view just the waveform,

  ut -v <signal_file>

  For example,

  ut -v vt.dump

Veritools

MODELTECH contd.

- To open the Undertow Suite in interactive mode, the command lines are as follows:
- ut -iv -modeltech <simulator_executable_name> <top level module names> "<simulator_options>" -sigfile <signal_filename> -ivsimcmp "-f<file that lists all source code files>"

  For example,

  ut -iv -modeltech vsim top -sigfile fsm.sigs -ivsimpcmp "-f source"

Veritools

STEPS FOR NCSIM

- Source environment variables

  For example,

  ./envsource

  --------------envsource file contents-------------------------------------

  #setenv CDS_INST_DIR <cadence installation directory>

  setenv CDS_INST_DIR /cad_tools/LDV5.1

  setenv ittsimUndertowSeDir $CDS_INST_DIR/tools/dfII/local/undertow

  setenv LD_LIBRARY_PATH /usr/lib/:usr/openwin/lib:$CDS_INST_DIR/tools/dfII/
  lib:$CDS_INST_DIR/tools/inca/lib:$CDS_INST_DIR/tools/lib:$CDS_INST_DIR/to
  ols/lib:$CDS_INST_DIR/tools/verilog/lib:/usr/dt/lib:/usr/lib/x11:/usr/ucblib:/usr2
  0/dt_cde/lib:/usr/local/lib/gcc-
  lib:/usr/local/lib:{SILOS}/bin:$UT_ROOT_DIR/PLI

  envsource contd.

Veritools

NCSIM contd.

envsource contd.

For Undertow versions 1.7 and up, please use the correct PLI according to the simulator
type and version.

$UT_ROOT_DIR has the following :

  ibpli.so.nc_verilog for NC Verilog . This is for CADENCE LDV versions 4.1, 5.1, 5.2
  and up libpli.so.old_nc_verilog for CADENCE LDV versions earlier than 4.1
  libpli.so.verilog_xl for Verilog-XL

Make sure you do the following:

  %cd $UT_ROOT_DIR/PLI/

  %cp <appropriate libpli.so.#> libpli.so

Also make sure LD_LIBRARY_PATH has $UT_ROOT_DIR/PLI in the path

- vt_veriuser.c and vtplinc.o are available in our PLI directory.

Veritools

NCSIM contd.

- <source> is the file that contains the source code files for Simulation
- To make the source file: add iv.v (in our distribution directory) at the top with top level file next followed by all the .v files needed in simulation
- Contents of iv.v file

  // iv.v

  module vtInteractive;

  initial

      $vtIv;

  endmodule

NCSIM contd.

- Add to source code close to top module

  initial

  begin

      $vtDumpvars(); /*dumps everything - created by our PLI routine.*/

  end
- In the example(in our distribution directory), the above has been inserted in 'top.v' file.

NCSIM contd.

- If you are compiling your design through the simulator for the first time, follow these steps:

   a) Run "ncprep"

   ncprep -f source

   -f <file> : used to specify file that contains all the user verilog files. Here, 'source' is
      a file with all of the user's Verilog files(top.v, fsm1.v, fsm2.v, fsm3.v) and iv.v

   iv.v is available in the example directory.

   Note that ncprep will generate the following files and directories.

   - cds.lib

   - hdl.vars

   - INCA_LIB

   - ncvlog.args

   - ncelab.args

   - ncsim.args

Veritools

NCSIM contd.

   b) Run "ncvlog"
   ncvlog -linedebug -f ncvlog.args
   c)Add the following line into file "ncleab.args"
   -ACCESS +RCW
   d) Run "ncelab"
   ncelab -f ncelab.args
   e) Run "ncsim"
   ncsim -f ncsim.args

Veritools

NCSIM contd.

- You can then compile through the simulator again as follows:

```
./run_ncsim
---------run_ncsim contents--------------------------------------------
#!/bin/csh -f
# Run the NC-Verilog parser (compile the source)
ncvlog -linedebug -f ncvlog.args
if ($status != 0) then
exit
Endif

# Run the NC-Verilog elaborator (build the design hierarchy)
ncelab -f ncelab.args
if ($status != 0) then
exit
Endif
```

run_ncsim *contd.*

Veritools

NCSIM contd.

```
run_ncsim  contd
# Run the NC-Verilog simulator (simulate the design)
#ncsim -f ncsim.args +VTCOMPRESS250 +VTVECTORVALUES
ncsim -f ncsim.args
-------------------------------------------------------------------------
NOTE: +VTCOMPRESS250 +VTVECTORVALUES will compress the size 0
```

Veritools

NCSIM contd.

- Viewing the NC Sim Waveform in batch mode, the commands are as follows:

  ut -iv -f <source_code_file> -sigfile <signal_file>

  source_code_file is the file that lists all the source code files.

  For example,

  ut -iv -f source -sigfile fsm.sigs

  To view just the waveform,

  ut -v <signal_file>

  For example,

  ut -v vt.dump

Veritools

NCSIM contd.

- Viewing the NC Sim Waveform in interactive mode, the commands are as follows

  a) Cadence Verilog-XL

  ut -iv -xl verilog -f <file that lists all source code filenames> -sigfile
      <signal_filename>

  For example,

  ut -iv -xl verilog -f source -sigfile fsm.sigs

  b) Cadence NC Verilog-XL

  ut -iv -ncxlmode ncxlmode -f <file that lists all source code filenames> -sigfile

  <signal_filename>

  For example,

  ut -iv -ncxlmode ncxlmode -f source -sigfile fsm.sigs

Veritools

NCSIM contd.

c) Cadence NC Verilog

ut -iv -nc ncverilog "-f <file that lists all source code filenames>" -sigfile
    <signal_filename>

For example,

ut -iv -nc ncverilog "-f source" -sigfile fsm.sigs

d) Cadence NC Sim (Compiled Simulator)

ut -iv -ncverilog ncsim "<simulator_options> -f ncsim.args" -sigfile
    <signal_filename> -ivsimcmp "-f <file that lists all source code file names>"

For example,

ut -iv -ncverilog ncsim "-f ncsim.args" -sigfile fsm.sigs -ivsimcmp "-f source"

OR

ut -iv -ncverilog ncsim worklib.top:v -sigfile fsm.sigs -ivsimcmp "-f source"

Veritools

Running Simulations
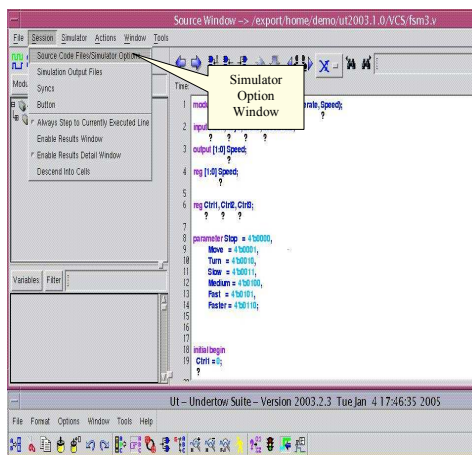
- After running the commands from the previous section to view those commands

- From the Source Code Window menu choose:

- Session => Source Code Files/Simulator Options

Veritools

Running Simulations contd.
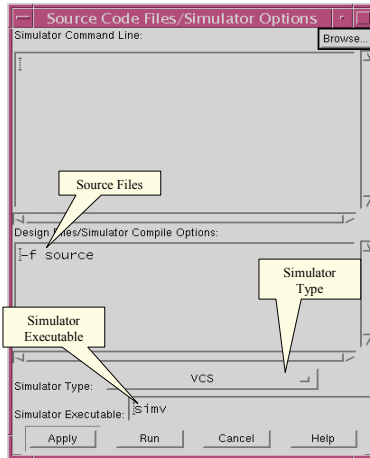
- Check for design files in the "Design Files/Simulator Compile Options:" text area and simulator executable in "Simulator Executable" text area
- Press Apply then Run
- Or from the Source Code Window menu choose:
- Simulator => Run
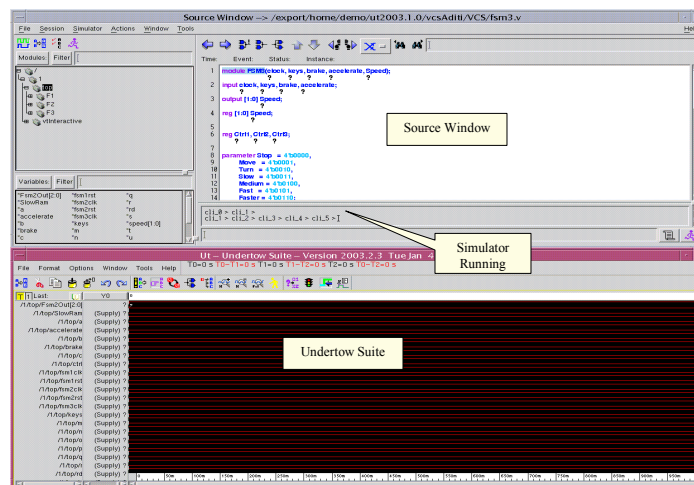
Running Simulations contd.

Running Simulations contd.
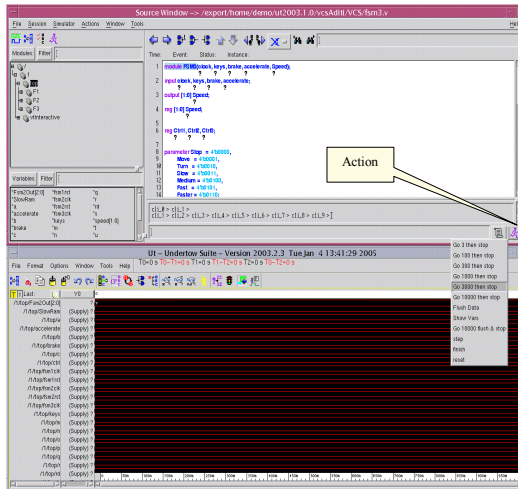
- Click on the "Action" button to display the list of commands for running the simulator
- Select "Go 3000 then stop"
- The simulator will run 3000 time points and stop
- This action has set the first break point at 3000 time point

Running Simulations contd.
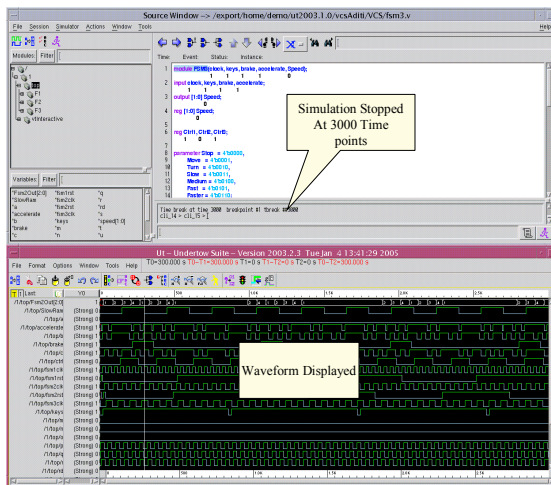
- To further run the simulator select the options from the "Action" button

"Action" Button
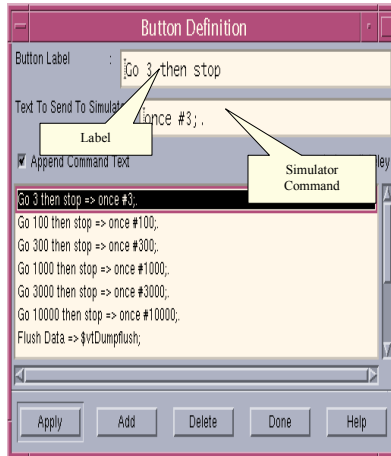
- To change the definition of the options in the "Action" list
- From the Source Code Window menu choose:
- Session => Button
- Print the text in "Button Label" text area and simulator command in "Text To Send To Simulator" text area in the "Button Definition" window
- Press Apply

Finish Simulation
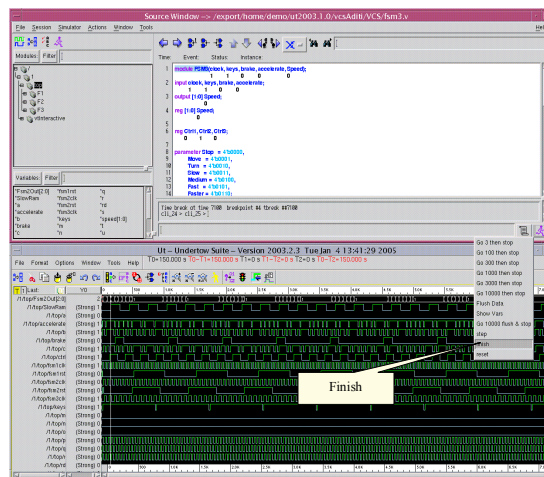
- To finish the simulation click on "Finish" from the "Action" list
- This will exit the simulator after it has finished the given time points
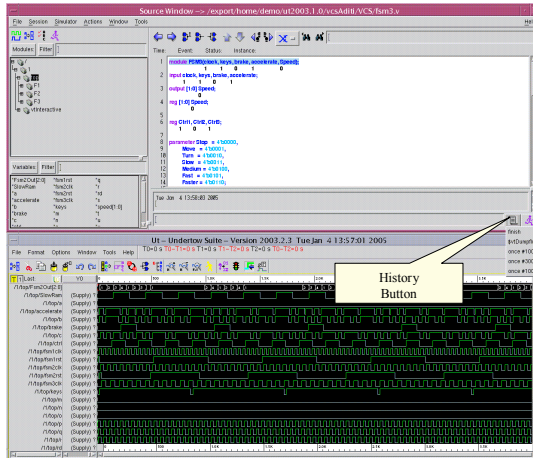
History

- Click on "History" button to display the list of previous executed commands.
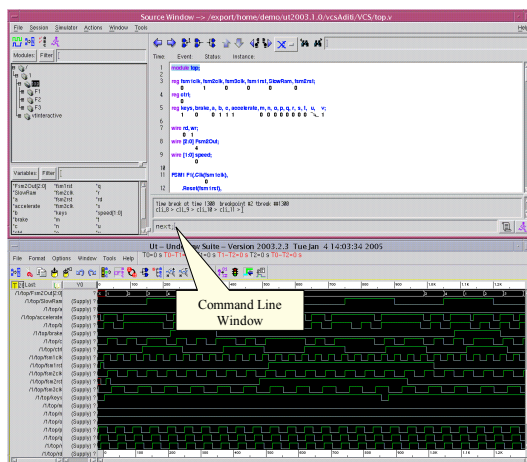
Command Line

- To type the commands for the simulator use command line window
- Press "Enter" after typing the command

Regaining the simulator
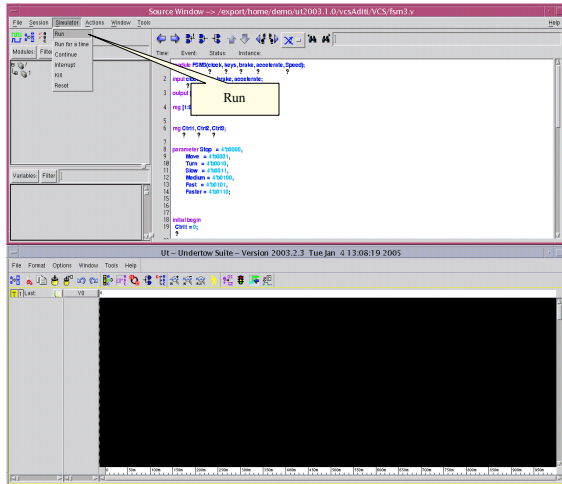
- To re-run the simulator after a simulation has exited
- From the Source Code Window menu choose:
- Simulator => Run
- This will restart the simulator from 0 time point
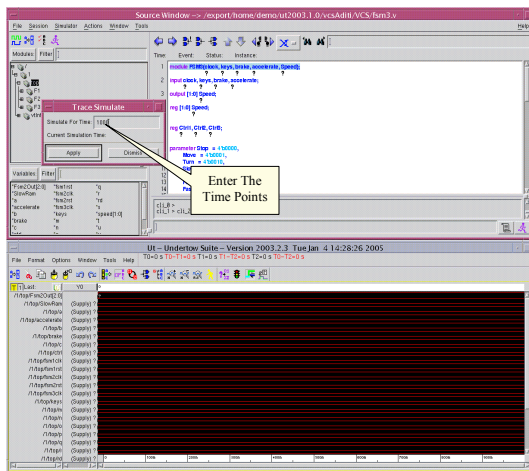
Run For

- To run the simulation for given time points
- From the Source Code Window menu choose:
- Simulator => Run For a Time
- Enter the time point in "Simulate For Time" text area and press "Apply"

Run For
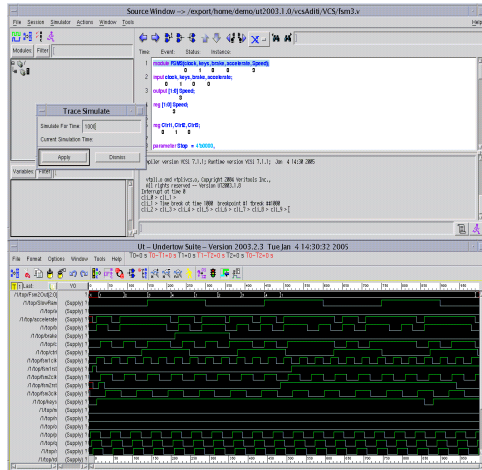
- This will run the simulator for the given time points and wait for next command
- This action has set the break point for the given time points
- To run the simulator without breakpoints type "." in the command line window and press "Enter"
- Or from the Source Code Window menu choose:
- Simulator => Continue

*V*eritools

Reset Simulator
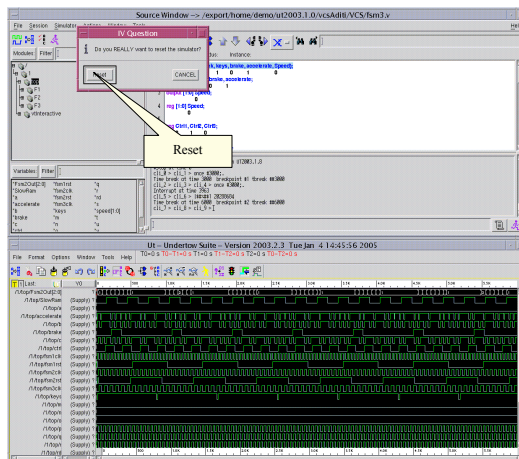
- To reset the simulator
- From the Source Code Window menu choose:
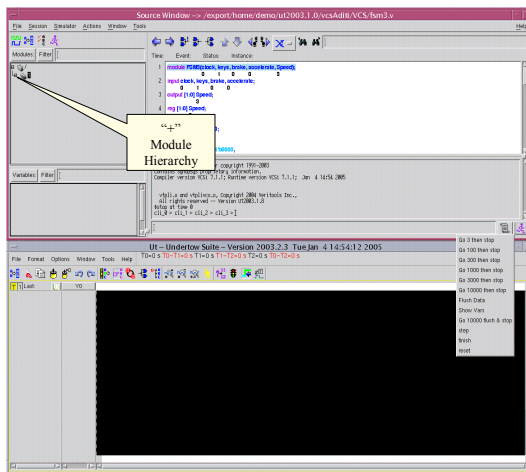- Simulator => Reset
- Press "Reset" in the "IV Question" window

*V*eritools

Reset Simulator
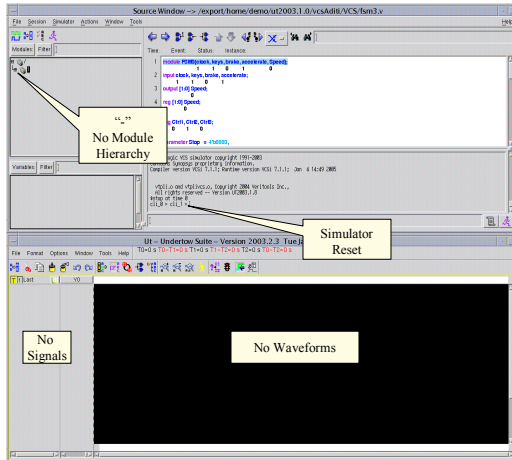
- This will reset the simulator
- After the simulator has been reset, to access module (signal) hierarchy, select the option to simulate for a giver amount of time, from the "Action" list or give a command from the command line window

Reset Simulator

- Giving the command to simulate for a given amount of time will give the access back to the module hierarchy

Stepping Source Code
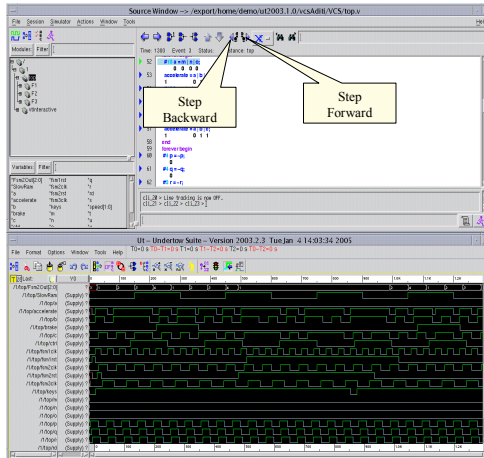
- Stepping the Source Code
- "Step Backward" will step back through the prior simulation steps that are in the trace file
- If you are at the last simulation time, clicking on "Step Forward" will step the simulation further

  If you are not at simulation "current time", stepping forward will step forward through simulation steps currently in the trace file.
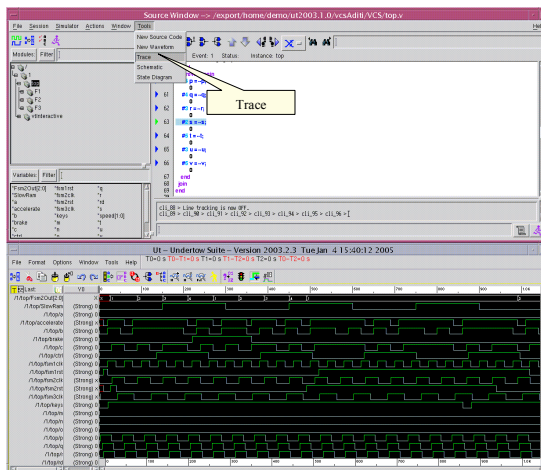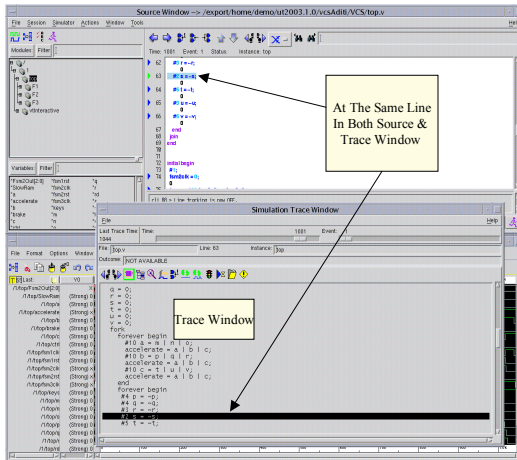
Trace Window

- To display the trace window
- From the Source Code Window menu choose:
- Tools => Trace

Trace Window

- The cursor on the trace window will point to the same line as the line of execution in the source code window
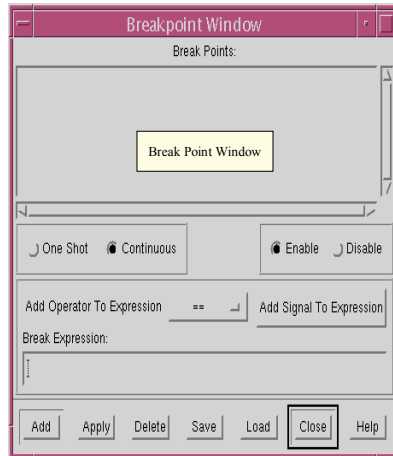
Setting Breakpoints
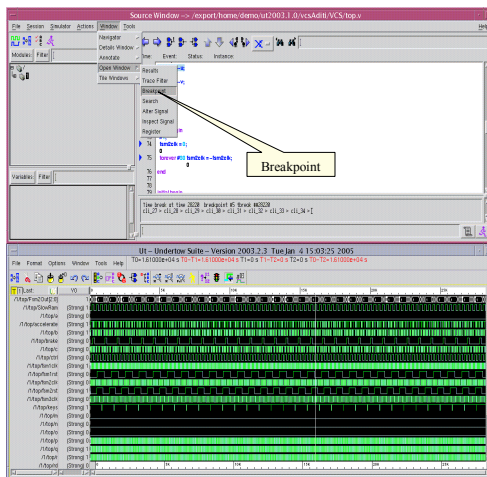
- To Set the breakpoint from the "Source Window"
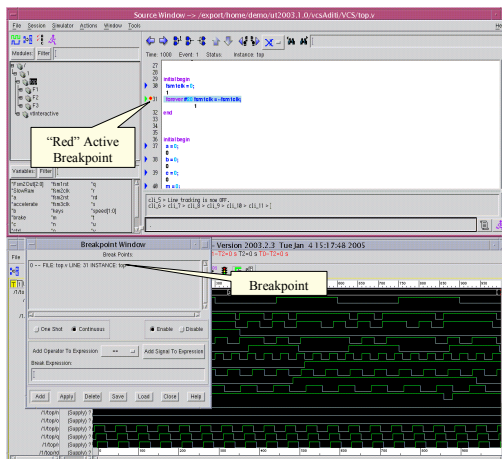- From the Source Code Window menu choose
- Window => Open Window -> Breakpoint
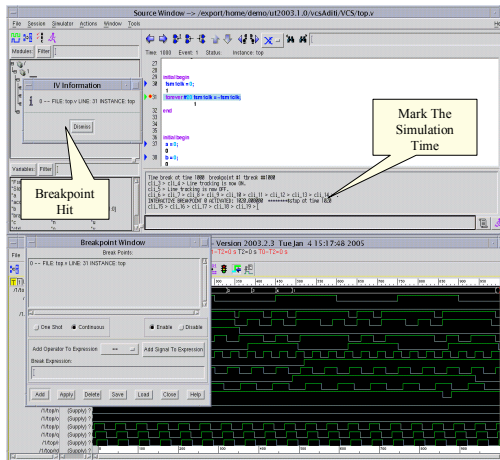
Veritools

Breakpoint Window

Adding Breakpoints

- To set the break point Left click the mouse button on the line number in the "Source Code Window"
- "Red" color will indicates an active break point
- The list of breakpoints will appear in the "Breakpoint Window"
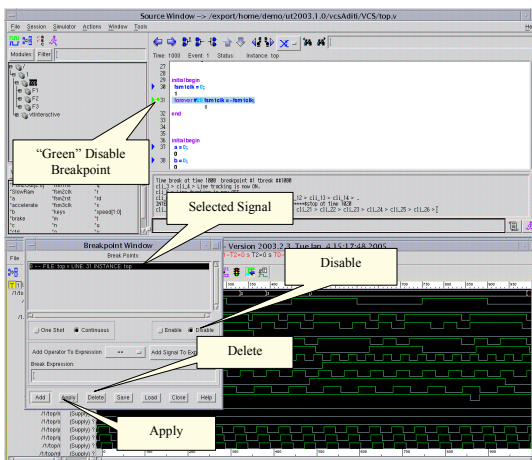
Adding Breakpoints

- Doing a continue by typing a "." in the command line
- Or from the Source Code Window menu choose Simulator => Continue will cause the simulator to stop at the break point

Veritools

Disable & Deleting Breakpoints

- To disable the breakpoint select the breakpoint in the "Breakpoint Window"
- Click on "Disable" button and then press "Apply"
- "Green" on the breakpoint line in the "Source Window" indicates disabled breakpoint
- To remove the breakpoint select the breakpoint in the "Breakpoint Window" and press "Delete"
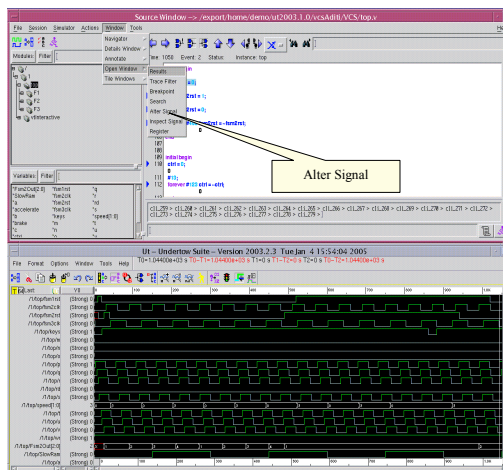
Veritools

One Shot Breakpoint
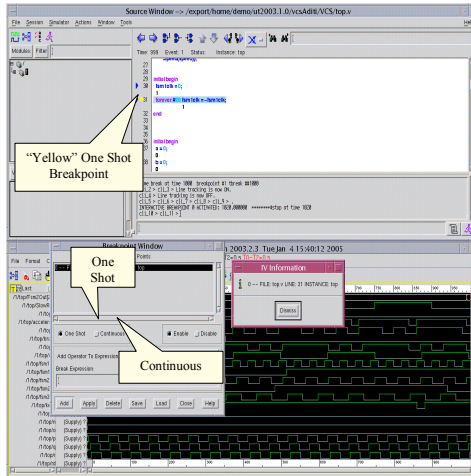
- "One Shot" allows the breakpoint to be hit only once during the given simulation time
- "Continuous" stops the simulation every time it reaches that breakpoint(default is "Continuous")
- To set the One Shot on the breakpoint select the breakpoint from the "Breakpoint Window" and select "One Shot" button
- "Yellow" indicates a One Shot break point
- If problem setting the One Shot toggle "Enable" and "Disable" buttons in the "Breakpoint Window"
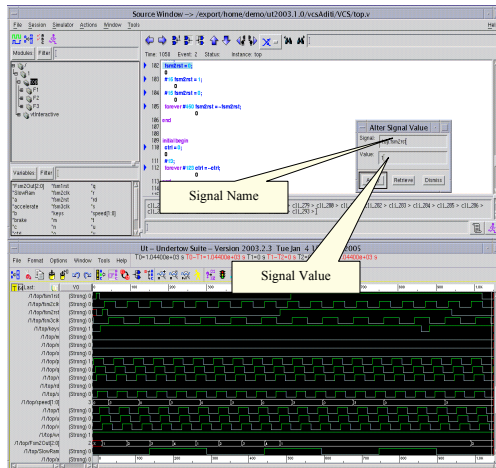
Alter Signal

- Alter Signal allows the user to change the current value of the signals for the proceeding simulations only
- From the Source Code Window menu choose
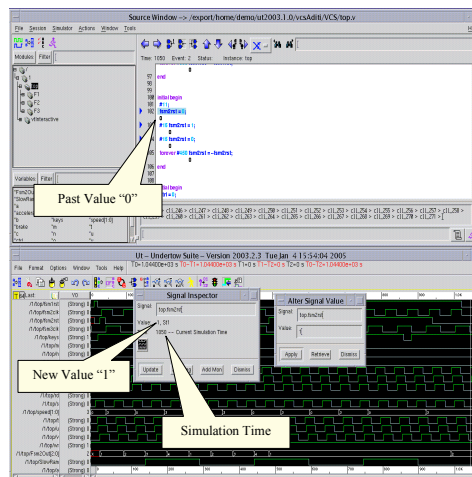- Window => Open Window -> Alter Signal

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Alter Signal

- Select the signal and drag and drop it in the text area for the "Signal" in the "Alter Signal Value" window
- Enter the new value for the signal for the proceeding simulations
- Press "Apply"

Signal Name

Signal Value

Inspect Signal

- To view the new changes in the value of the signal
- From the Source Code Window menu choose
- Window => Open Window -> Inspect Signal
- Select the signal and drag and drop it in the text area for the "Signal" in the "Signal Inspector" window
- Press "Update"
- The new value of the signal at the current time will be displayed

Past Value "0"

New Value "1"
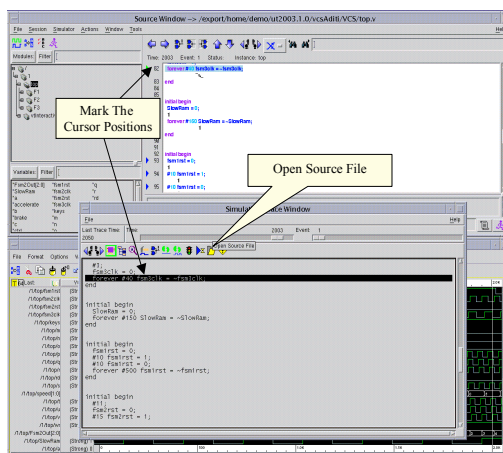
Simulation Time
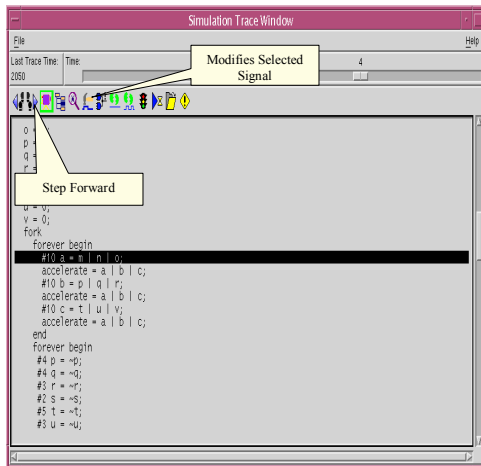
Trace Window

- "Simulation Trace Window" allows to move to next simulation point by using "Step Forward" button if you are at the last simulation time point
- Or to move backward in the past simulation time by using "Step Backward"
- To move forward in the past simulation use "Step Forward"
- If the simulator is running and last time point in simulation is reached clicking on "Step Forward" will advance the simulation one step further
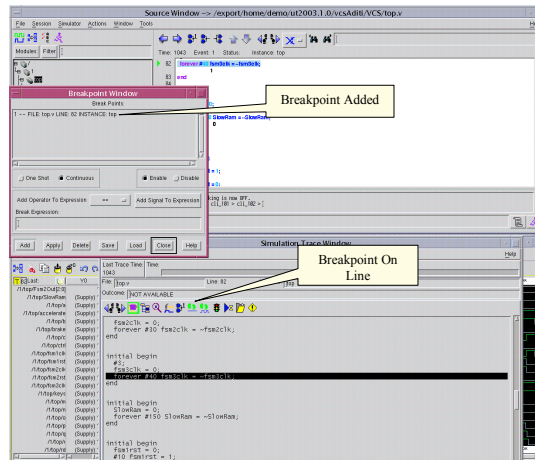

Source & Trace Window Synchronization

- To force the "Source Window" to be at the same point in simulation as "Trace Window" click on "Open Source File" button
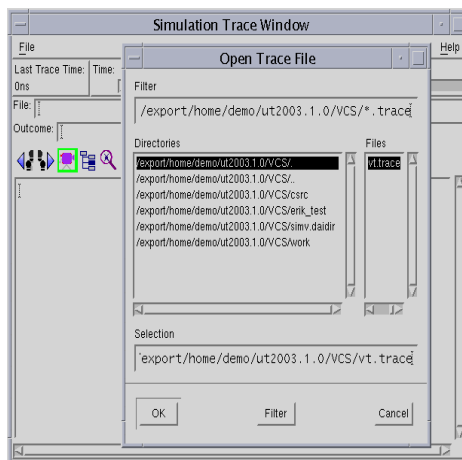
Trace - Breakpoints

- To add the breakpoint in the "Simulation Trace Window" at the given cursor position
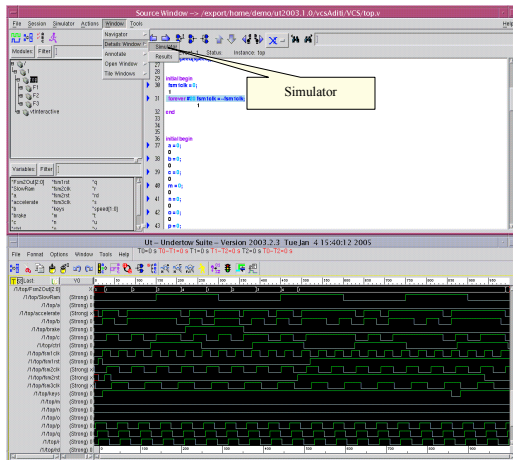- Click in "Breakpoint On Line" button

Veritools

Virtual Trace

- To view the trace file when the simulation is not running
- From the Simulation Trace Window menu choose:
- File => Open Trace File …
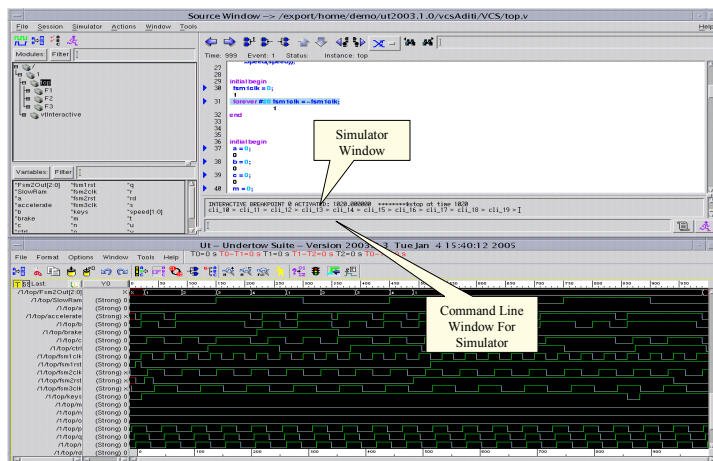- Select the desired ".trace" file and click "Ok"

Veritools

Simulator Window

- To view the Simulator Window in the "Source Window"
- From the Source Window menu choose:
- Window => Details Window -> Simulator

Veritools

Simulator Window

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- End of Using Simulator with Undertow Suite tutorial …

Go back to the Main Menu

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