



Veritools

Using Simulator With
Undertow Suite

Veritools

STEPS FOR SIMULATING USING VCS:



- Source environment variables

For example, envsource has all the environment variables set up.

You can change the paths accordingly.

-----envsource file contents-----

```
setenv VCSI_HOME <path where VCSI is installed>
```

```
setenv DEFAULT_VCS_HOME <path where VCSI is installed>
```

```
setenv VCS_HOME <path where VCSI is installed>
```

```
setenv TMPDIR /tmp
```

```
setenv VCS_NETHOST vt1
```

```
setenv VCS_LTD_LICENSE 1
```

```
setenv VCS_CC cc
```

- vtplivcs.o and vt_vcs.tab are present in our PLI directory

VCS contd.



- `<source>` is the file that contains the source code files for Simulation
- To make the source file: add `iv.v` (found in our distribution directory) at the top with top level file next followed by all the `.v` files needed in simulation.
- Contents of `iv.v` file

```
// iv.v
module vtInteractive;
initial
    $vtIv;
endmodule
```

VCS cont.



- Add to source code close to top module

```
initial
begin
    $vtDumpvars(); /*dumps everything - created by our PLI routine.*/
    $vtTrace(1) /*enables event tracing of your complete design*/
end
```
- In the example(in our distribution directory), the above has been inserted in 'top.v' file.

VCS cont.



- To compile through the simulator in interactive mode do as follows:
vcsi <flags> -f source \$UT_ROOT_DIR/PLI/vtplivcs.o -P
\$UT_ROOT_DIR/PLI/vt_vcs.tab
- For example,
./run_vcsi_int
-----run_vcsi_int contents-----
#!/bin/csh -f
vcsi -Mupdate +vpi +cli +acc+2 -lm -line -f source
\$UT_ROOT_DIR/PLI/vtplivcs.o -P UT_ROOT_DIR/PLI/vt_vcs.tab

VCS cont.



- To open the Undertow Suite in batch mode, the command lines is as follows:
ut -iv -f <source> -sigfile <dump filename>
<source> is the file that contains the source code files for simulation
For example,
ut -iv -f source -sigfile fsm.sigs -tracefile fsm.trace
To view just the waveform,
ut -v <signal_file>
For example,
ut -v vt.dump
- To open the Undertow Suite in interactive mode the command lines is as follows:
ut -iv -vcs <vcs_simulator_executable> <simulator_options> -sigfile
<signal_filename> -tracefile <trace_filename> -ivsimcmp "-f <file that lists
all source code file names>"
For example,
ut -iv -vcs simv -sigfile fsm.sigs -tracefile fsm.trace -ivsimpcmp "-f source"

STEPS FOR SIMULATING USING MODELTECH



- Sourcing environment Variables

For example,

`./envsource`

-----envsource file contents-----

`setenv PLIOBJS $UT_ROOT_DIR/PLI/vtpli_modtech.so`

`setenv ModelTech <path where ModelTech has been installed>`

- `vtpli_modtech.so` is available in our PLI directory.

MODELTECH contd.



- <source> is the file that contains the source code files for Simulation
- To make the source file: add iv.v at the top with top level file next followed by all the .v files needed in simulation followed by “+libverbose” at the bottom.

- Contents of iv.v file

```
// iv.v
module vtInteractive;
initial
    $vtIv;
endmodule
```


MODELTECH contd.



- Add to source code close to top module

```
initial
begin
    $vtDumpvars(); /*dumps everything - created by our PLI routine.*/
end
```
- In the example(in our distribution directory), the above has been inserted in 'top.v' file.

MODELTECH contd.



- Compile through the simulator as follows:

```
./run_modeltech
```

```
run_modeltech : script for running all modelsim commands.
```

```
-----run_modeltech contents-----
```

```
#!/bin/csh -f
```

```
if (-e work) then
```

```
    rm -r -f work
```

```
endif
```

```
if (! -e work) then
```

```
    vlib work #creates new design library work
```

```
endif
```

```
vlog -f source #compiles the verilog files into the work library
```

```
vsim -c -do 'run -all' top vtInteractive +VTCOMPRESS250 +VTVECTORVALUES
```

MODELTECH contd.



- To open the Undertow Suite in batch mode, the command lines are as follows:

```
ut -iv -f <source_code_file> -sigfile <signal_file>
```

<source_code_file> is the file that lists all the source code files.

For example,

```
ut -iv -f source -sigfile fsm.sigs
```

To view just the waveform,

```
ut -v <signal_file>
```

For example,

```
ut -v vt.dump
```

MODELTECH contd.



- To open the Undertow Suite in interactive mode, the command lines are as follows:
- `ut -iv -modeltech <simulator_executable_name> <top level module names> <simulator_options> -sigfile <signal_filename> -ivsimcmp "-f<file that lists all source code files>"`

For example,

```
ut -iv -modeltech vsim top -sigfile fsm.sigs -ivsimpcmp "-f source"
```

STEPS FOR SIMULATING USING NCSIM



- Source environment variables

For example,

```
./envsource
```

```
-----envsource file contents-----
```

```
#setenv CDS_INST_DIR <cadence installation directory>
```

```
setenv CDS_INST_DIR /cad_tools/LDV5.1
```

```
setenv ittSimUndertowSeDir $CDS_INST_DIR/tools/dfII/local/undertow
```

```
setenv LD_LIBRARY_PATH /usr/lib:/usr/openwin/lib:$CDS_INST_DIR/tools/dfII/  
lib:$CDS_INST_DIR/tools/inca/lib:$CDS_INST_DIR/tools/lib:$CDS_INST_DIR/to  
ols/
```

```
lib:$CDS_INST_DIR/tools/verilog/lib:/usr/dt/lib:/usr/lib/x11:/usr/ucblib:/usr20/dt_c  
de/lib:/usr/
```

```
local/lib/gcc-lib:/usr/local/lib:{SILOS}/bin:$UT_ROOT_DIR/PLI
```

envsource contd.

NCSIM contd.



envsource contd.

For Undertow versions 1.7 and up, please use the correct PLI according to the simulator type and version.

`$UT_ROOT_DIR` has the following :

`ibpli.so.nc_verilog` for NC Verilog . This is for CADENCE LDV versions 4.1, 5.1, 5.2 and up
`libpli.so.old_nc_verilog` for CADENCE LDV versions earlier than 4.1

`libpli.so.verilog_xl` for Verilog-XL

Make sure you do the following:

```
%cd $UT_ROOT_DIR/PLI/
```

```
%cp <appropriate libpli.so.> libpli.so
```

Also make sure `LD_LIBRARY_PATH` has `$UT_ROOT_DIR/PLI` in the path

- `vt_veriuser.c` and `vtplinc.o` are available in our PLI directory.

NCSIM contd.



- <source> is the file that contains the source code files for Simulation
- To make the source file: add iv.v (in our distribution directory) at the top with top level file next followed by all the .v files needed in simulation

- Contents of iv.v file

```
// iv.v
```

```
module vtInteractive;
```

```
initial
```

```
    $vtIv;
```

```
endmodule
```

NCSIM contd.



- Add to source code close to top module

```
initial
begin
    $vtDumpvars(); /*dumps everything - created by our PLI routine.*/
end
```
- In the example(in our distribution directory), the above has been inserted in 'top.v' file.

NCSIM contd.



- If you are compiling your design through the simulator for the first time, follow these steps:

a) Run "ncprep"

```
ncprep -f source
```

-f <file> : used to specify file that contains all the user verilog files. Here, 'source' is a file with all of the user's Verilog files(top.v, fsm1.v, fsm2.v, fsm3.v) and iv.v
iv.v is available in the example directory.

Note that ncprep will generate the following files and directories.

- cds.lib
- hdl.vars
- INCA_LIB
- ncvlog.args
- ncelab.args
- ncsim.args

NCSIM contd.



b) Run "ncvlog"

```
ncvlog -f ncvlog.arg
```

c) Add the following line into file "ncleab.args"

```
-ACCESS +RCW
```

d) Run "ncelab"

```
ncelab -f ncelab.args
```

e) Run "ncsim"

```
ncsim -f ncsim.args
```

NCSIM contd.



- You can then compile through the simulator again as follows:

```
./run_ncsim
-----run_ncsim contents-----
#!/bin/csh -f
# Run the NC-Verilog parser (compile the source)
ncvlog -f ncvlog.args
if ($status != 0) then
  exit
Endif

# Run the NC-Verilog elaborator (build the design hierarchy)
ncelab -f ncelab.args
if ($status != 0) then
  exit
Endif
```

run_ncsim *contd.*

NCSIM contd.



```
run_ncsim contd
```

```
# Run the NC-Verilog simulator (simulate the design)
```

```
#ncsim -f ncsim.args +VTCOMPRESS250 +VTVECTORVALUES
```

```
ncsim -f ncsim.args
```

NOTE: +VTCOMPRESS250 +VTVECTORVALUES will compress the size 0

NCSIM contd.



- Viewing the NC Sim Waveform in batch mode, the commands are as follows:

```
ut -iv -f <source_code_file> -sigfile <signal_file>
```

source_code_file is the file that lists all the source code files.

For example,

```
ut -iv -f source -sigfile fsm.sigs
```

To view just the waveform,

```
ut -v <signal_file>
```

For example,

```
ut -v vt.dump
```

NCSIM contd.



- Viewing the NC Sim Waveform in interactive mode, the commands are as follows

a) Cadence Verilog-XL

```
ut -iv -xl verilog -f <file that lists all source code filenames> -sigfile  
  <signal_filename>
```

For example,

```
ut -iv -xl verilog -f source -sigfile fsm.sigs
```

b) Cadence NC Verilog-XL

```
ut -iv -ncxlm mode ncxlm mode -f <file that lists all source code filenames> -sigfile  
  <signal_filename>
```

For example,

```
ut -iv -ncxlm mode ncxlm mode -f source -sigfile fsm.sigs
```

NCSIM contd.



c) Cadence NC Verilog

```
ut -iv -nc ncverilog "-f <file that lists all source code filenames>" -sigfile  
    <signal_filename>
```

For example,

```
ut -iv -nc ncverilog "-f source" -sigfile fsm.sigs
```

d) Cadence NC Sim (Compiled Simulator)

```
ut -iv -ncverilog ncsim "-f ncsim.args" -sigfile <signal_filename> -ivsimcmp "-f  
    <file that lists all source code file names>"
```

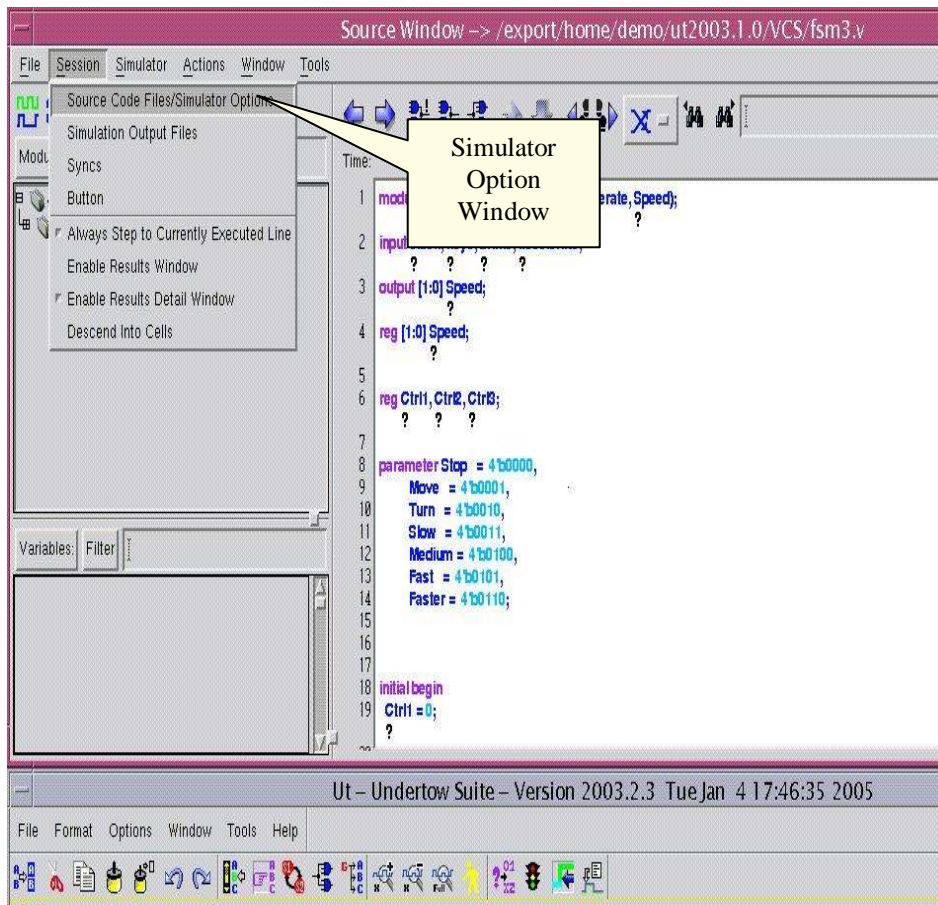
For example,

```
ut -iv -ncverilog ncsim "-f ncsim.args" -sigfile fsm.sigs -ivsimcmp "-f source"
```

OR

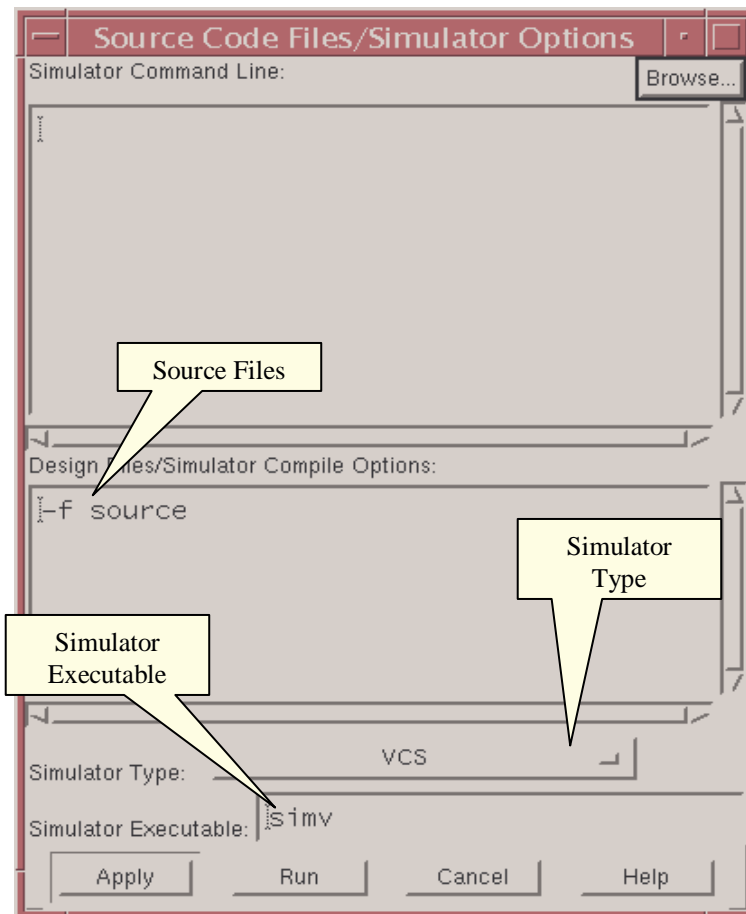
```
ut -iv -ncverilog ncsim worklib.top:v -sigfile fsm.sigs -ivsimcmp "-f source"
```

Running Simulations



- After running the commands from the previous section to view those commands
- From the Source Code Window menu choose:
- Session => Source Code Files/Simulator Options

Running Simulations contd.



- Check for design files in the “Design Files/Simulator Compile Options:” text area and simulator executable in “Simulator Executable” text area
- Press Apply then Run
- Or from the Source Code Window menu choose:
- Simulator => Run

Running Simulations contd.

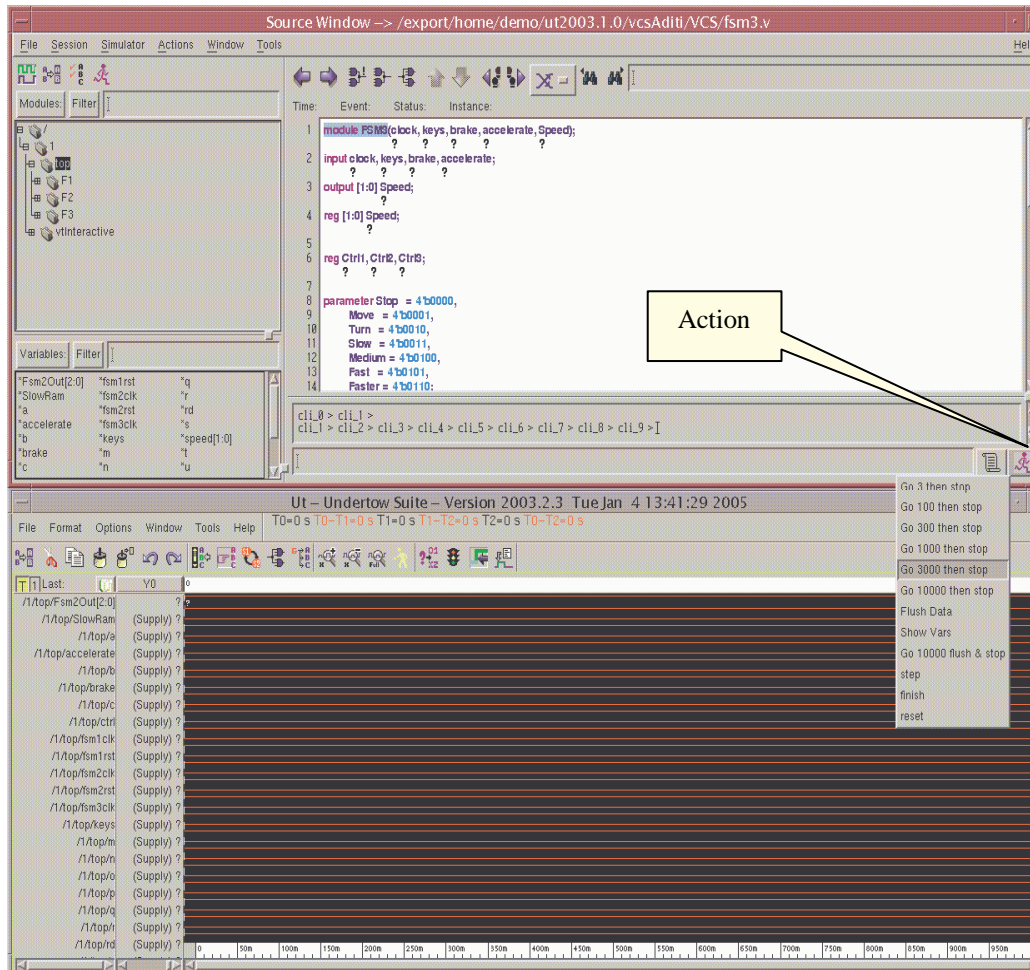


The screenshot displays the Veritools simulation environment. The top window, titled "Source Window", shows the Verilog code for a module named "FSM3". The code includes inputs for clock, keys, brake, and accelerate, and an output for Speed. It also defines a register for Speed and control signals (Ctrl1, Ctrl2, Ctrl3). Parameters for Stop, Move, Turn, Slow, Medium, and Fast are defined. The code is as follows:

```
1 module FSM3(clock, keys, brake, accelerate, Speed);
2 input clock, keys, brake, accelerate;
3 output [1:0] Speed;
4 reg [1:0] Speed;
5
6 reg Ctrl1, Ctrl2, Ctrl3;
7
8 parameter Stop = 4'b0000,
9           Move = 4'b0001,
10          Turn = 4'b0010,
11          Slow = 4'b0011,
12          Medium = 4'b0100,
13          Fast = 4'b0101,
14          Faster = 4'b0110;
15
16 cli_0 > cli_1 >
17 cli_1 > cli_2 > cli_3 > cli_4 > cli_5 >]
```

The bottom window, titled "Ut - Undertow Suite - Version 2003.2.3 Tue Jan 4", shows the simulator running. The left pane displays a list of modules and their instances, including "Fsm2Out", "SlowRam", "accelerate", "brake", "c", "Fsm1rst", "Fsm2clk", "Fsm2rst", "Fsm3clk", "keys", "m", "n", "q", "r", "rd", "s", "speed[1:0]", and "u". The right pane shows the simulation results, which are currently blank. A callout box labeled "Simulator Running" points to the simulator window. Another callout box labeled "Source Window" points to the code editor. A third callout box labeled "Undertow Suite" points to the simulation results pane.

Running Simulations contd.



- Click on the “Action” button to display the list of commands for running the simulator
- Select “Go 3000 then stop”
- The simulator will run 3000 time points and stop
- This action has set the first break point at 3000 time point

Running Simulations contd.



The screenshot displays the Veritools simulation environment. The top window, titled "Source Window", shows the source code for a module named "FSM3". The code includes module declarations, input/output signals, registers, and parameters. A yellow callout box points to the code with the text "Simulation Stopped At 3000 Time points". The bottom window, titled "Ut - Undertow Suite - Version 2003.2.3", shows a waveform display for various signals. A yellow callout box points to the waveform with the text "Waveform Displayed".

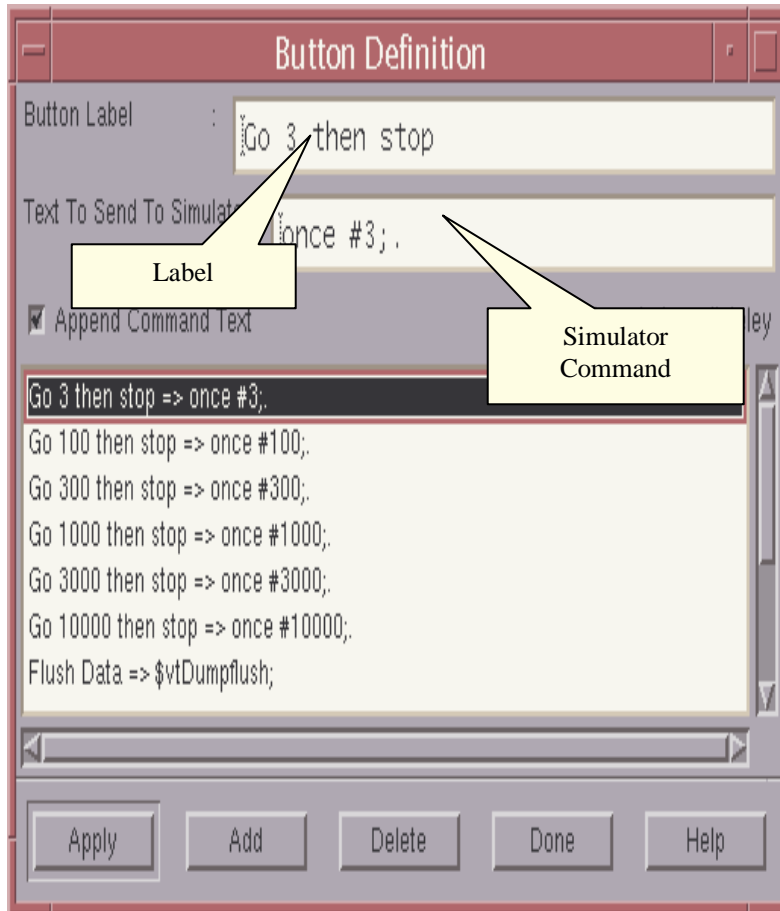
```
1 module FSM3(clock, keys, brake, accelerate, Speed);
2   input clock, keys, brake, accelerate;
3   output [1:0] Speed;
4   reg [1:0] Speed;
5
6   reg Ctrl1, Ctrl2, Ctrl3;
7
8   parameter Stop = 4'b0000,
9             Move = 4'b0001,
10            Turn = 4'b0010,
11            Slow = 4'b0011,
12            Medium = 4'b0100,
13            Fast = 4'b0101,
14            Faster = 4'b0110;
```

Time break at time 3000 breakpoint #1 tbreak ##3000
cli_14 > cli_15 >]

Waveform signals include: /!top/Fsm2Out[2:0], /!top/SlowRam, /!top/a, /!top/accelerate, /!top/b, /!top/brake, /!top/c, /!top/ctrl, /!top/fsm1clk, /!top/fsm1rst, /!top/fsm2clk, /!top/fsm2rst, /!top/fsm3clk, /!top/keys, /!top/m, /!top/n, /!top/o, /!top/p, /!top/q, /!top/r, /!top/rd.

- To further run the simulator select the options from the “Action” button

“Action” Button



- To change the definition of the options in the “Action” list
- From the Source Code Window menu choose:
- Session => Button
- Print the text in “Button Label” text area and simulator command in “Text To Send To Simulator” text area in the “Button Definition” window
- Press Apply

Finish Simulation



Source Window -> /export/home/demo/ut2003.1.0/vcsAditi/VCS/fsm3.v

```
1 module FSM3(clock, keys, brake, accelerate, Speed);
2   input clock, keys, brake, accelerate;
3   output [1:0] Speed;
4   reg [1:0] Speed;
5
6   reg Ctrl1, Ctrl2, CtrlB;
7
8   parameter Stop = 4'b0000,
9     Move = 4'b0001,
10    Turn = 4'b0010,
11    Slow = 4'b0011,
12    Medium = 4'b0100,
13    Fast = 4'b0101,
14    Faster = 4'b0110;

```

Time: Event: Status: Instance:

Time break at time 7100 breakpoint #4 tbreak ##7100
cli_24 > cli_25 > |

Ut - Undertow Suite - Version 2003.2.3 Tue Jan 4 13:41:29 2005
T0=150.000 s T0-T1=150.000 s T1=0 s T1-T2=0 s T2=0 s T0-T2=150.000 s

Finish

- To finish the simulation click on “Finish” from the “Action” list
- This will exit the simulator after it has finished the given time points

History



The screenshot displays the Veritools simulation environment. The top window, titled "Source Window", shows the source code for a module named "FSM3". The code includes declarations for inputs (clock, keys, brake, accelerate), outputs (Speed), registers (Ctrl1, Ctrl2, Ctrl3), and parameters (Stop, Move, Turn, Slow, Medium, Fast, Faster). The bottom window, titled "Ut - Undertow Suite", shows a timing diagram with multiple signals. A yellow callout box with the text "History Button" points to a button in the bottom right corner of the source window.

- Click on “History” button to display the list of previous executed commands.

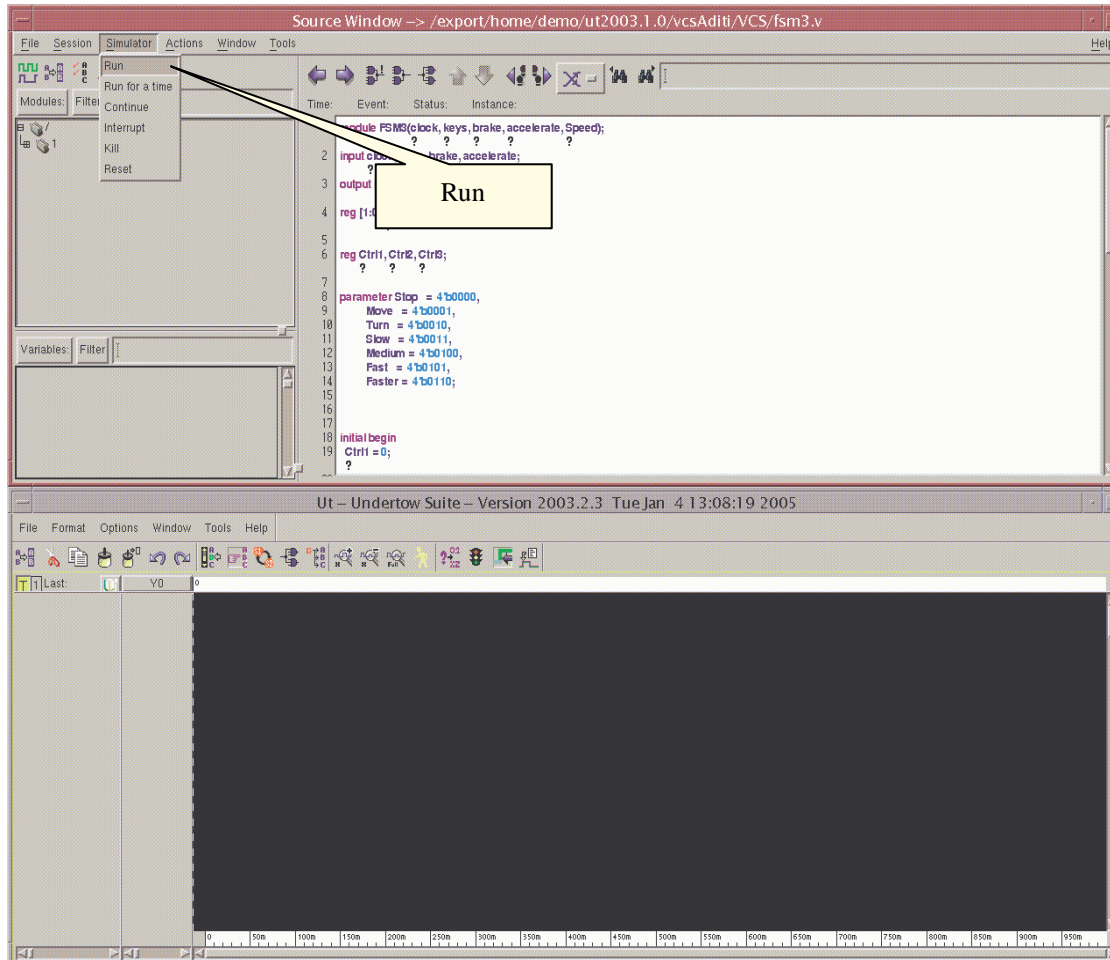
Command Line



The screenshot displays the Veritools simulation environment. The top window, titled "Source Window", shows the Verilog code for a module named "top". The code includes registers for fsm1clk, fsm2clk, fsm3clk, fsm1rst, SlowRam, fsm2rst, and ctrl; a reg ctr; a reg keys, brake, a, b, c, accelerate, m, n, o, p, q, r, s, t, u, v; wires rd, wr; wire [2:0] Fsm2Out; wire [1:0] speed; an FSM1 F1 with clock fsm1clk and reset fsm1rst; and a .Reset! fsm1rst; statement. A time break is set at time 1300 with a breakpoint #2 and a break #1300. The command line window shows the command: `cli_0 > cli_9 > cli_10 > cli_11 >`. The bottom window, titled "Timing Diagram", shows a list of signals on the left and their waveforms on the right. A yellow callout box labeled "Command Line Window" points to the command line window in the timing diagram.

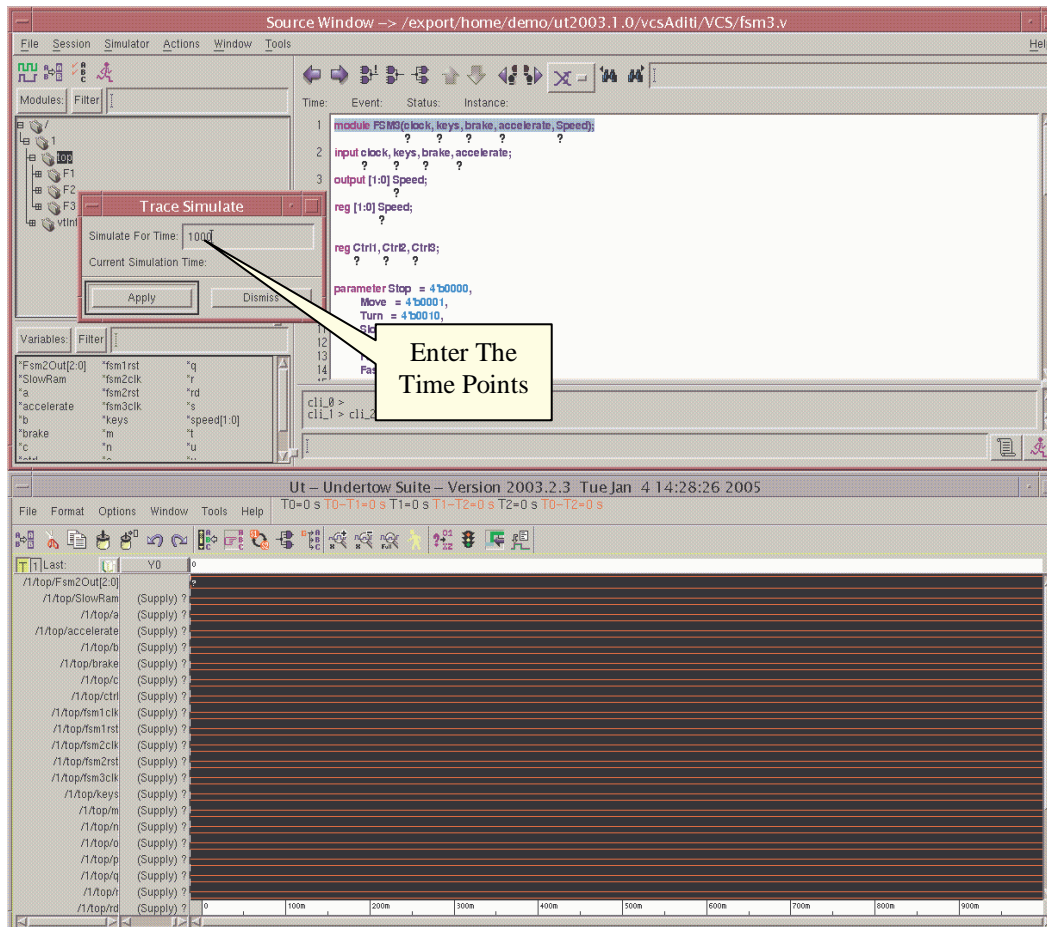
- To type the commands for the simulator use command line window
- Press “Enter” after typing the command

Regaining the simulator



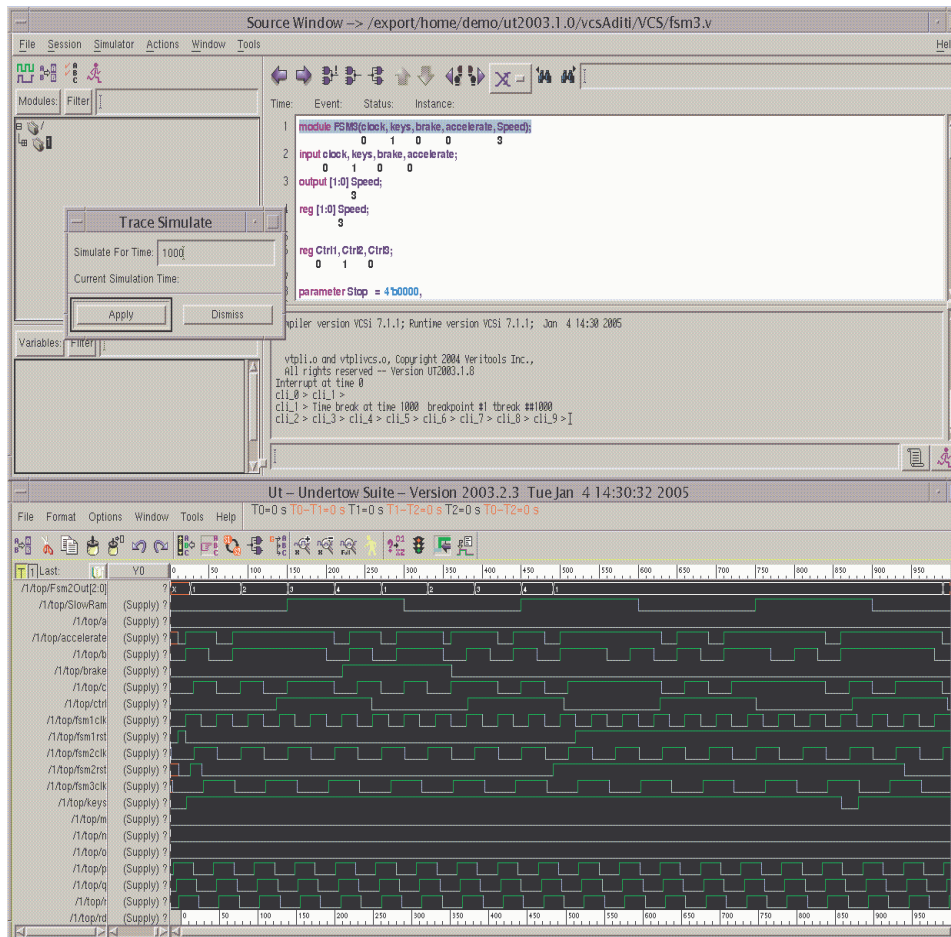
- To re-run the simulator after a simulation has exited
- From the Source Code Window menu choose:
- Simulator => Run
- This will restart the simulator from 0 time point

Run For



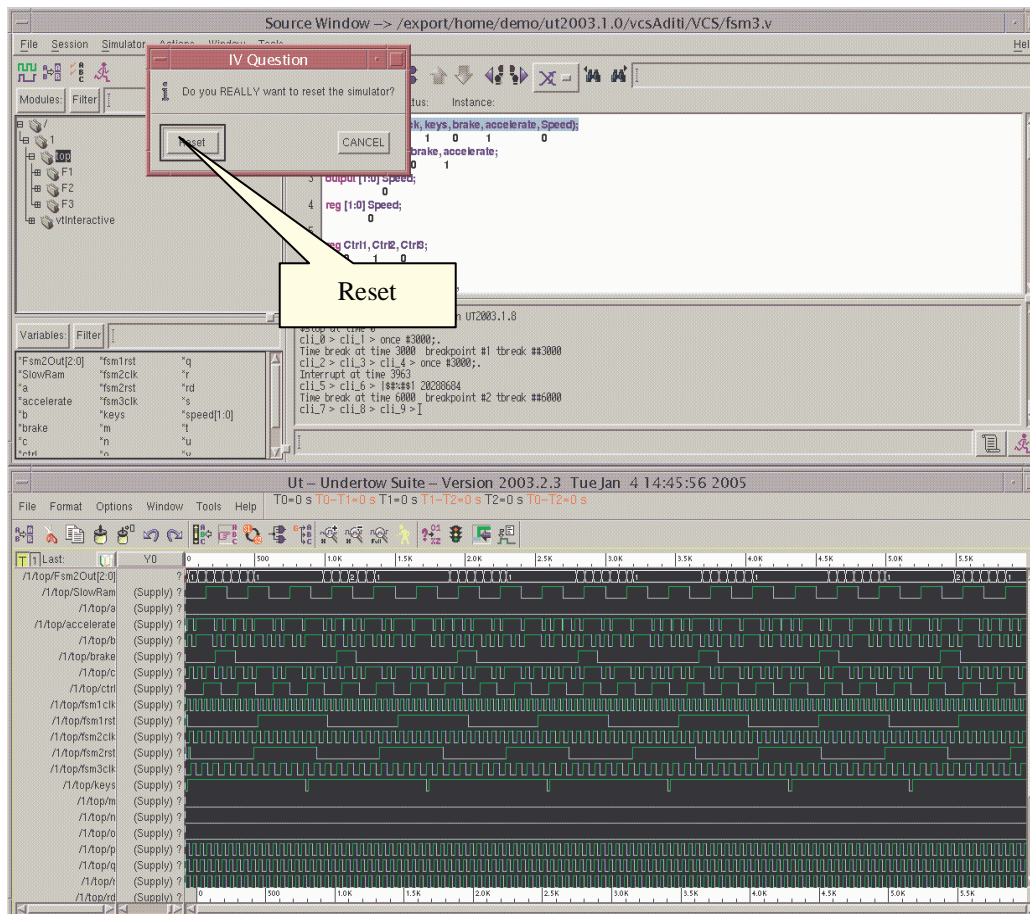
- To run the simulation for given time points
- From the Source Code Window menu choose:
- Simulator => Run For a Time
- Enter the time point in “Simulate For Time” text area and press “Apply”

Run For



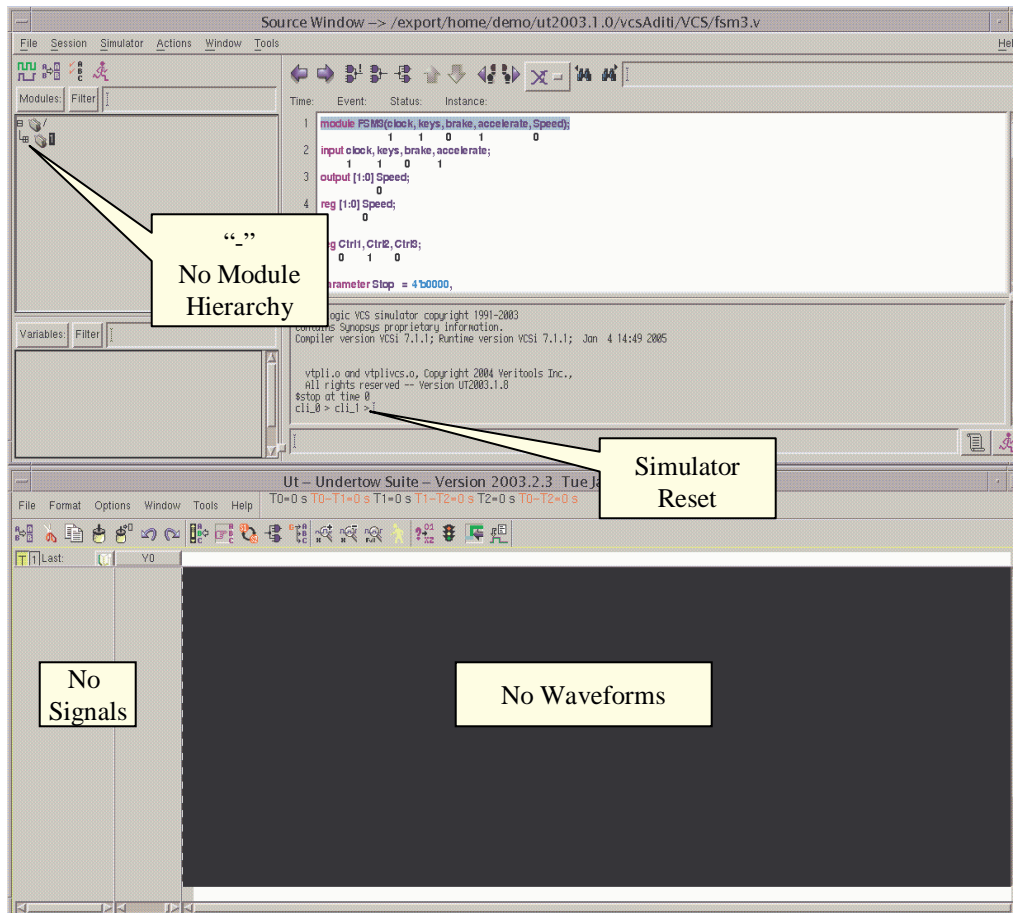
- This will run the simulator for the given time points and wait for next command
- This action has set the break point for the given time points
- To run the simulator without breakpoints type “.” in the command line window and press “Enter”
- Or from the Source Code Window menu choose:
- Simulator => Continue

Reset Simulator



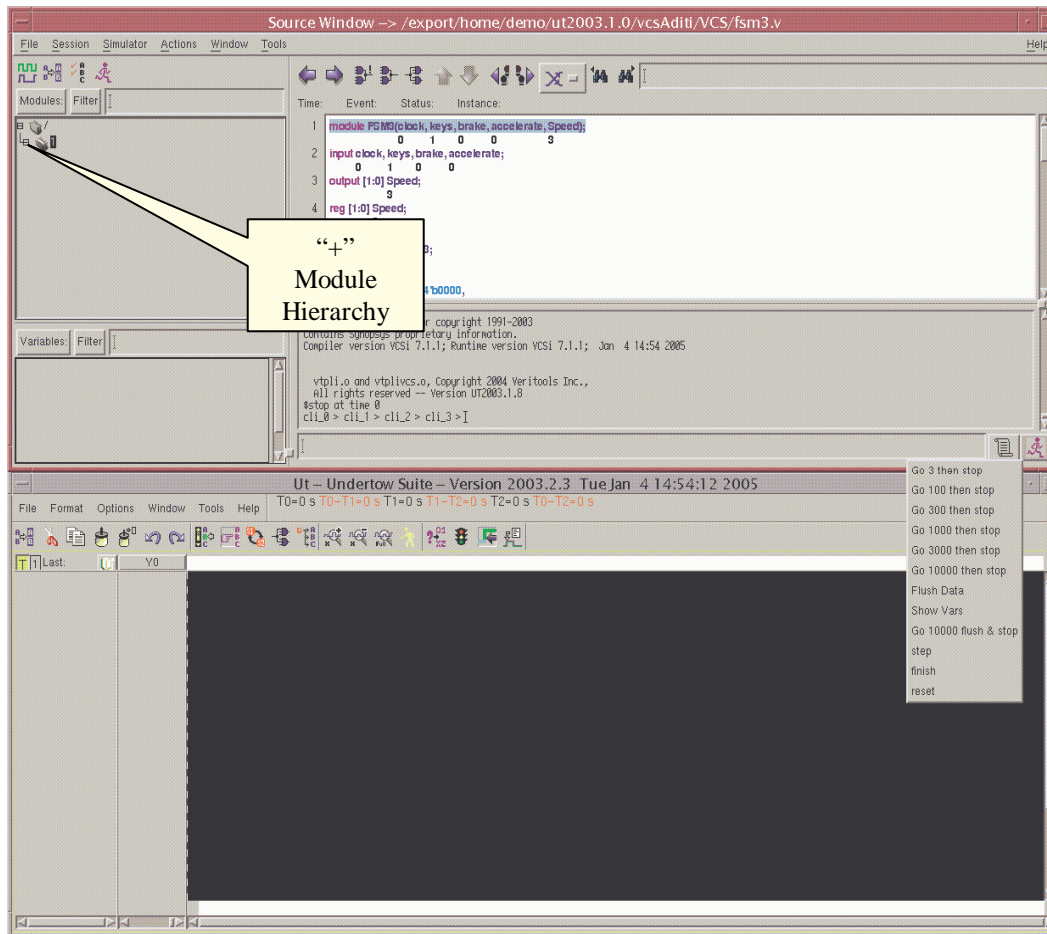
- To reset the simulator
- From the Source Code Window menu choose:
 - Simulator => Reset
- Press "Reset" in the "IV Question" window

Reset Simulator



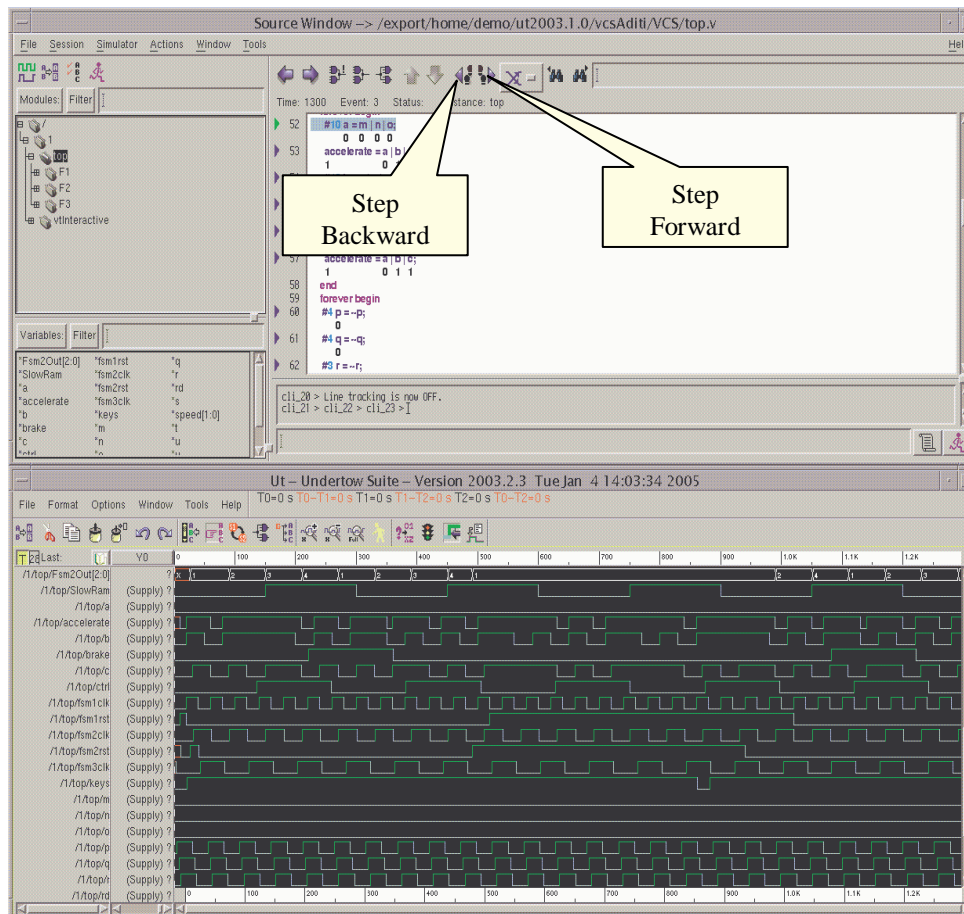
- This will reset the simulator
- After the simulator has been reset, to access module (signal) hierarchy, select the option to simulate for a given amount of time, from the “Action” list or give a command from the command line window

Reset Simulator



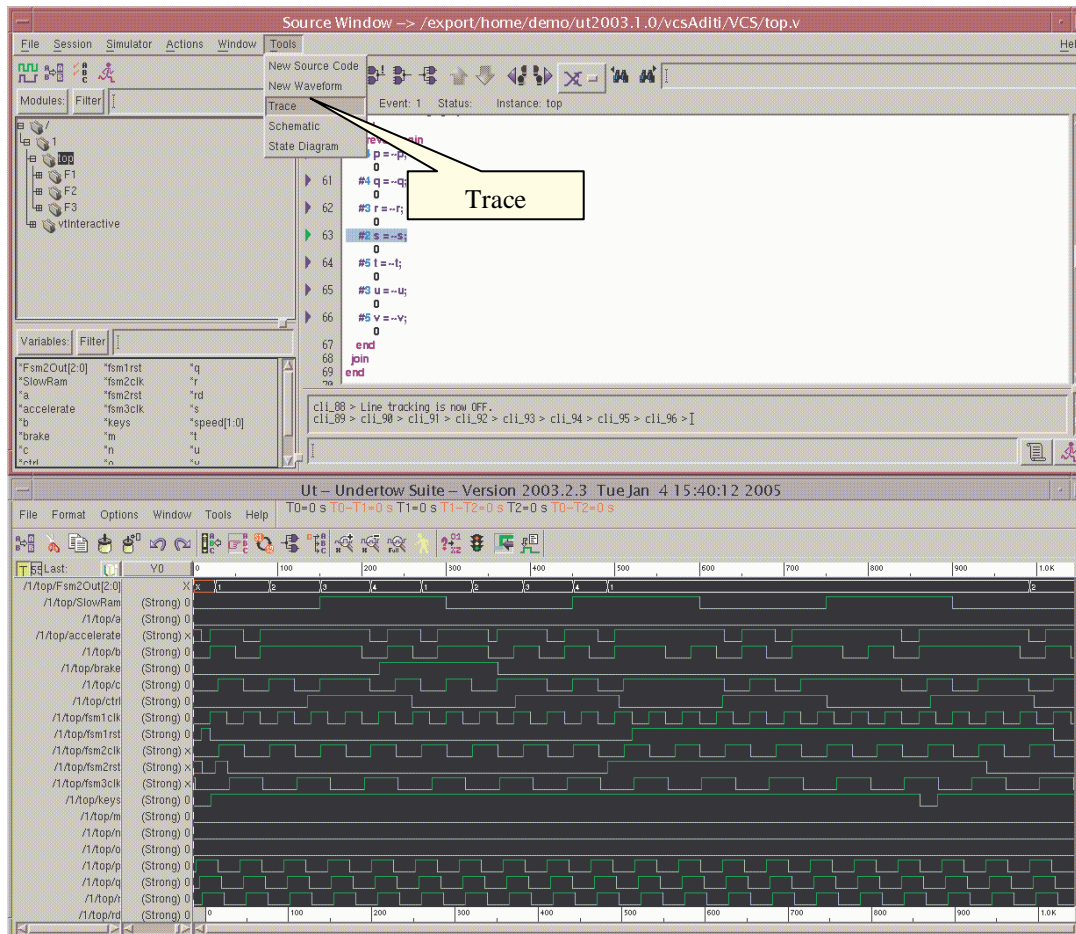
- Giving the command to simulate for a given amount of time will give the access back to the module hierarchy

Stepping Source Code



- Stepping the Source Code
 - “Step Backward” will step back through the prior simulation steps that are in the trace file
 - If you are at the last simulation time, clicking on “Step Forward” will step the simulation further
- If you are not at simulation “current time”, stepping forward will step forward through simulation steps currently in the trace file.

Trace Window



- To display the trace window
- From the Source Code Window menu choose:
- Tools => Trace

Trace Window



The screenshot displays the Veritools interface with two windows open:

- Source Window:** Shows the source code for `/export/home/demo/ut2003.1.0/vcsAedit/VCS/top.v`. Line 63 is highlighted in blue. The code includes:

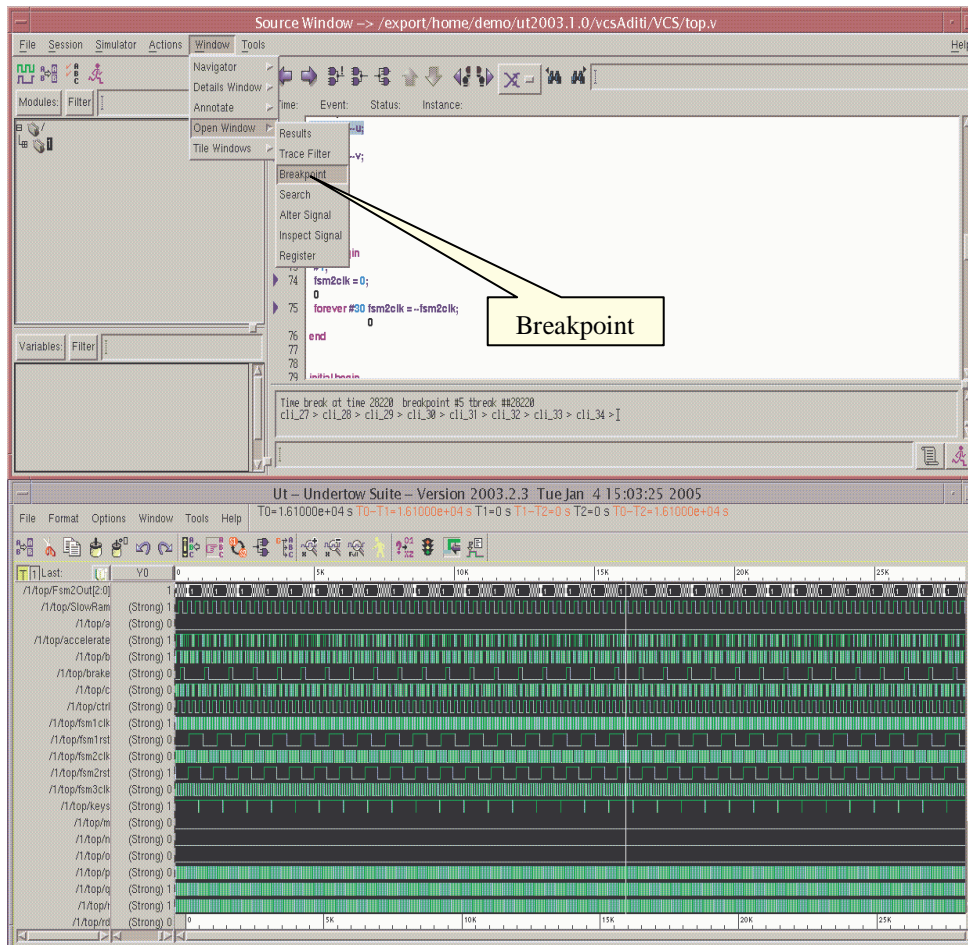
```
62 #3 r = ~r;  
63 #5 s = ~s;  
64 #5 l = ~l;  
65 #3 u = ~u;  
66 #5 v = ~v;  
67 #5  
68 join  
69 end  
70  
71  
72 initial begin  
73 #1;  
74 fsm2clk = 0;  
75 #5  
76  
77 r1: r > 1 line tracking is now OFF.
```
- Simulation Trace Window:** Shows the simulation trace for the same file and instance. Line 63 is also highlighted in blue. The trace output includes:

```
q = 0;  
r = 0;  
s = 0;  
t = 0;  
u = 0;  
v = 0;  
fork  
  forever begin  
    #10 a = m | n | o;  
    accelerate = a | b | c;  
    #10 b = p | q | r;  
    accelerate = a | b | c;  
    #10 c = t | u | v;  
    accelerate = a | b | c;  
  end  
  forever begin  
    #4 d = ~d;  
    #4 q = ~q;  
    #3 r = ~r;  
    #2 s = ~s;  
    #5 t = ~t;
```

Two yellow callout boxes with arrows point to the corresponding line 63 in both windows. The top box contains the text "At The Same Line In Both Source & Trace Window". The bottom box contains the text "Trace Window".

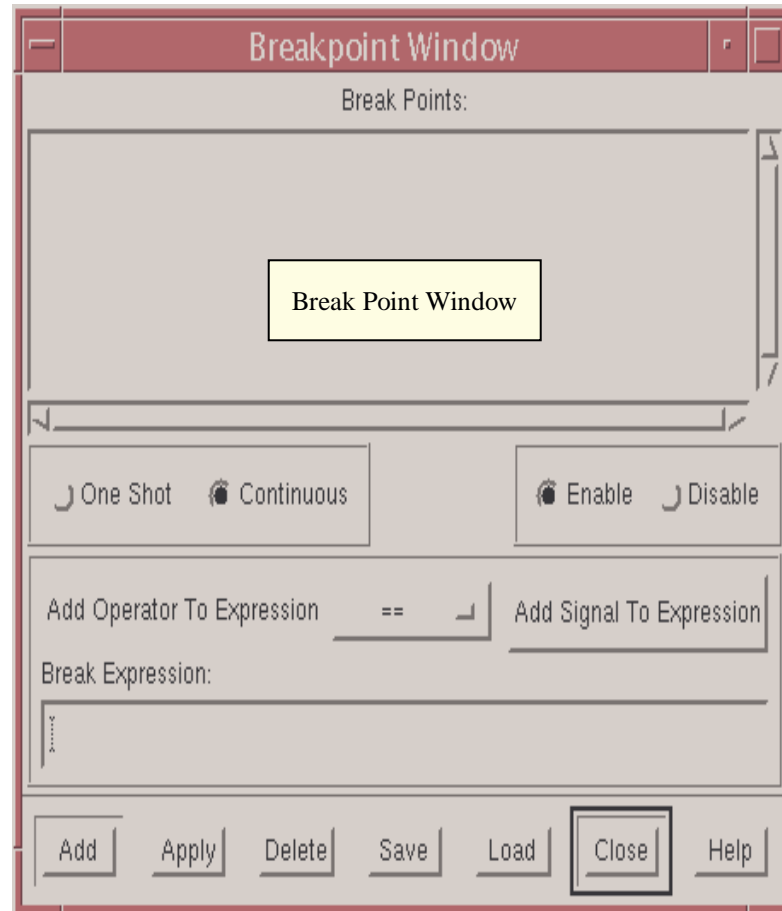
- The cursor on the trace window will point to the same line as the line of execution in the source code window

Setting Breakpoints



- To Set the breakpoint from the “Source Window”
- From the Source Code Window menu choose
- Window => Open Window -> Breakpoint

Breakpoint Window



Adding Breakpoints



The screenshot displays two windows from the Veritools IDE. The top window, titled "Source Window", shows a Verilog code snippet with a red arrow pointing to line 31, which contains the statement `forever #20 fsm1clk = ~fsm1clk;`. A callout box labeled "Red" Active Breakpoint" points to this line. The bottom window, titled "Breakpoint Window", shows a list of breakpoints and a timing diagram. A callout box labeled "Breakpoint" points to the first entry in the list, which is `0 -- FILE: top.v LINE: 31 INSTANCE: top`. The timing diagram shows several digital signals over time, with a red vertical line indicating the current breakpoint position.

- To set the break point
Left click the mouse button on the line number in the “Source Code Window”
- “Red” color will indicate an active breakpoint
- The list of breakpoints will appear in the “Breakpoint Window”

Adding Breakpoints



The screenshot displays the Veritools simulation environment. The top window, titled 'Source Window', shows a Verilog code snippet with a breakpoint set at line 31: `forever #20 fsm1clk = ~fsm1clk;`. A yellow callout box points to this line with the text 'Mark The Simulation Time'. Below the code, a console window shows the simulation output, including a message: 'Time break at time 1000 breakpoint #1 tbreak ##1000'. A yellow callout box points to this message with the text 'Breakpoint Hit'. The bottom window, titled 'Breakpoint Window', shows the configuration for the breakpoint, including options for 'One Shot' and 'Continuous', and a 'Break Expression' field. To the right, a waveform window displays a digital signal trace over time, with a vertical marker indicating the breakpoint at 1000 ns.

- Doing a continue by typing a “.” in the command line
- Or from the Source Code Window menu choose Simulator => Continue will cause the simulator to stop at the break point

Disable & Deleting Breakpoints



The screenshot shows the Veritools Source Window and Breakpoint Window. The Source Window displays a Verilog code snippet with a breakpoint set at line 31. A yellow callout box labeled "Green" Disable Breakpoint points to the green line number 31. The Breakpoint Window shows the breakpoint configuration for line 31, with a yellow callout box labeled "Selected Signal" pointing to the signal list. The Breakpoint Window also has a "Disable" button and a "Delete" button, both highlighted with yellow callout boxes. The "Apply" button is also highlighted with a yellow callout box. The Breakpoint Window shows the breakpoint is currently disabled.

- To disable the breakpoint select the breakpoint in the “Breakpoint Window”
- Click on “Disable” button and then press “Apply”
- “Green” on the breakpoint line in the “Source Window” indicates disabled breakpoint
- To remove the breakpoint select the breakpoint in the “Breakpoint Window” and press “Delete”

One Shot Breakpoint



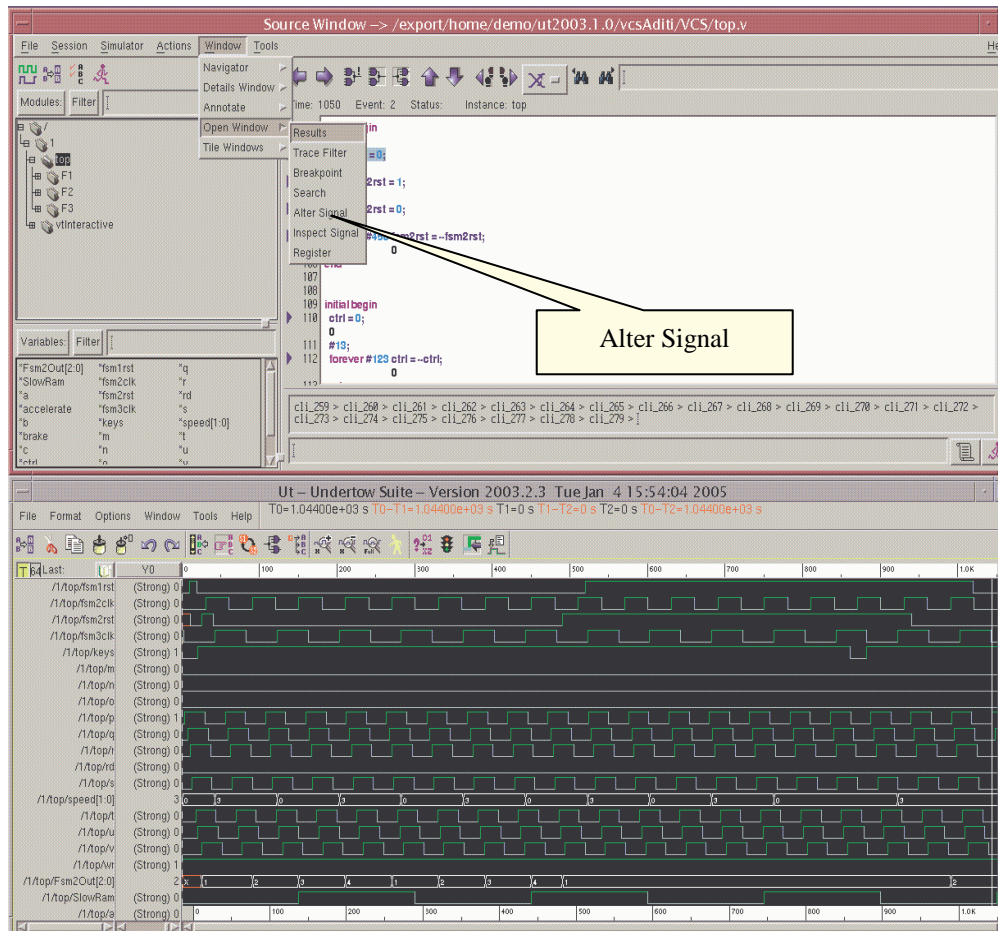
The screenshot displays the Veritools interface. The top window, 'Source Window', shows a code editor with the following code:

```
27 //specify;
28
29 initial begin
30   fsm_talk = 0;
31   forever #10 fsm_talk = ~fsm_talk;
32   1
33 end
34
35 initial begin
36   a = 0;
37   0
38   b = 0;
39   0
```

A yellow callout points to line 31, labeled "Yellow One Shot Breakpoint". The 'Breakpoint Window' below shows a list of breakpoints with 'One Shot' selected for the breakpoint at line 31. A yellow callout points to this selection, labeled 'One Shot'. The 'Breakpoint Window' also has 'Continuous' selected, with a yellow callout pointing to it, labeled 'Continuous'. A 'Dismiss' dialog box is visible over the waveform window.

- “One Shot” allows the breakpoint to be hit only once during the given simulation time
- “Continuous” stops the simulation every time it reaches that breakpoint (default is “Continuous”)
- To set the One Shot on the breakpoint select the breakpoint from the “Breakpoint Window” and select “One Shot” button
- “Yellow” indicates a One Shot breakpoint
- If problem setting the One Shot toggle “Enable” and “Disable” buttons in the “Breakpoint Window”

Alter Signal



- Alter Signal allows the user to change the current value of the signals for the proceeding simulations only
- From the Source Code Window menu choose
- Window => Open Window -> Alter Signal

Alter Signal



The screenshot shows the Veritools Source Window with the following Verilog code:

```
102 fsm2rst = 0;
103 #15 fsm2rst = 1;
104 #15 fsm2rst = 0;
105 forever #450 fsm2rst = ~fsm2rst;
106 end
107
108
109 initial begin
110 ctrl = 0;
111 #15;
112 forever #125 ctrl = ~ctrl;
113 end
```

The 'Alter Signal Value' dialog box is open, showing:

- Signal: fsm2rst
- Value: 1

Callouts indicate that the 'Signal' field is the 'Signal Name' and the 'Value' field is the 'Signal Value'.

- Select the signal and drag and drop it in the text area for the “Signal” in the “Alter Signal Value” window
- Enter the new value for the signal for the proceeding simulations
- Press “Apply”

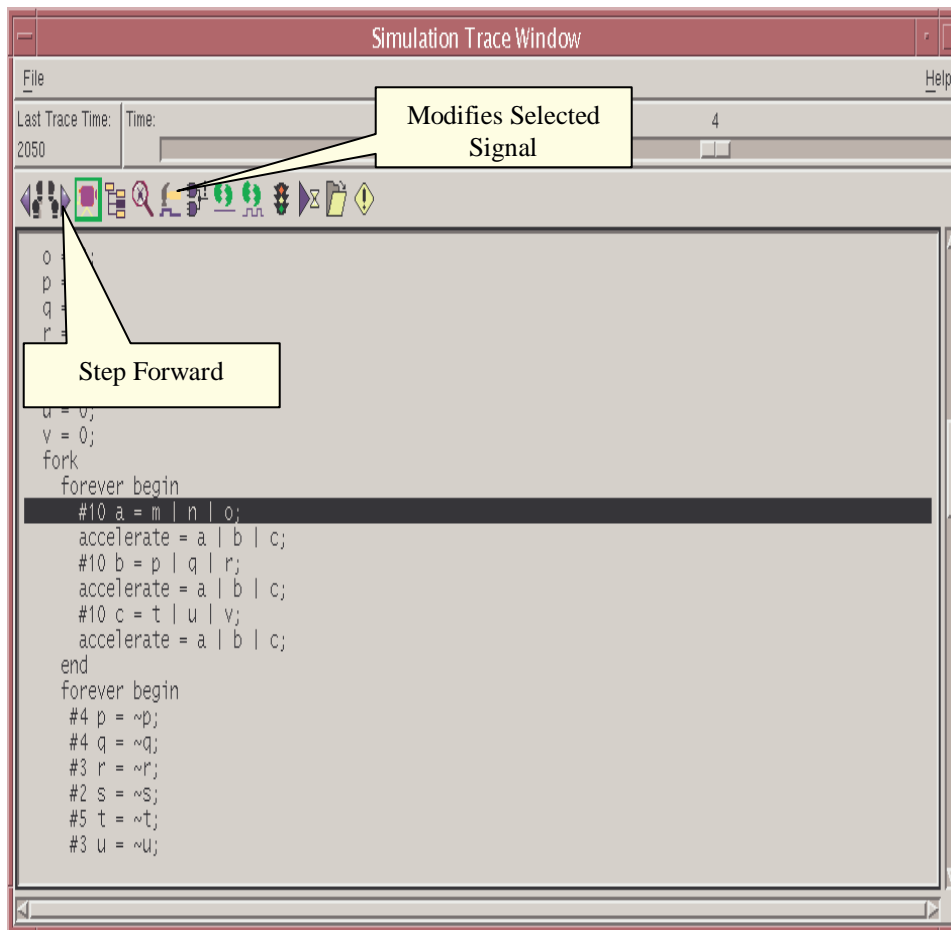
Inspect Signal



The screenshot displays the Veritools simulation environment. The top window shows the source code for a Verilog module. A yellow callout points to the line `fsm2rst = 0;` with the text "Past Value '0'". The bottom window shows the Signal Inspector and a waveform viewer. A yellow callout points to the "Value" field in the Signal Inspector, which contains "1, S11", with the text "New Value '1'". Another yellow callout points to the "1050 -- Current Simulation Time" field in the Signal Inspector with the text "Simulation Time". The waveform viewer shows a digital signal that has transitioned from 0 to 1 at the current simulation time.

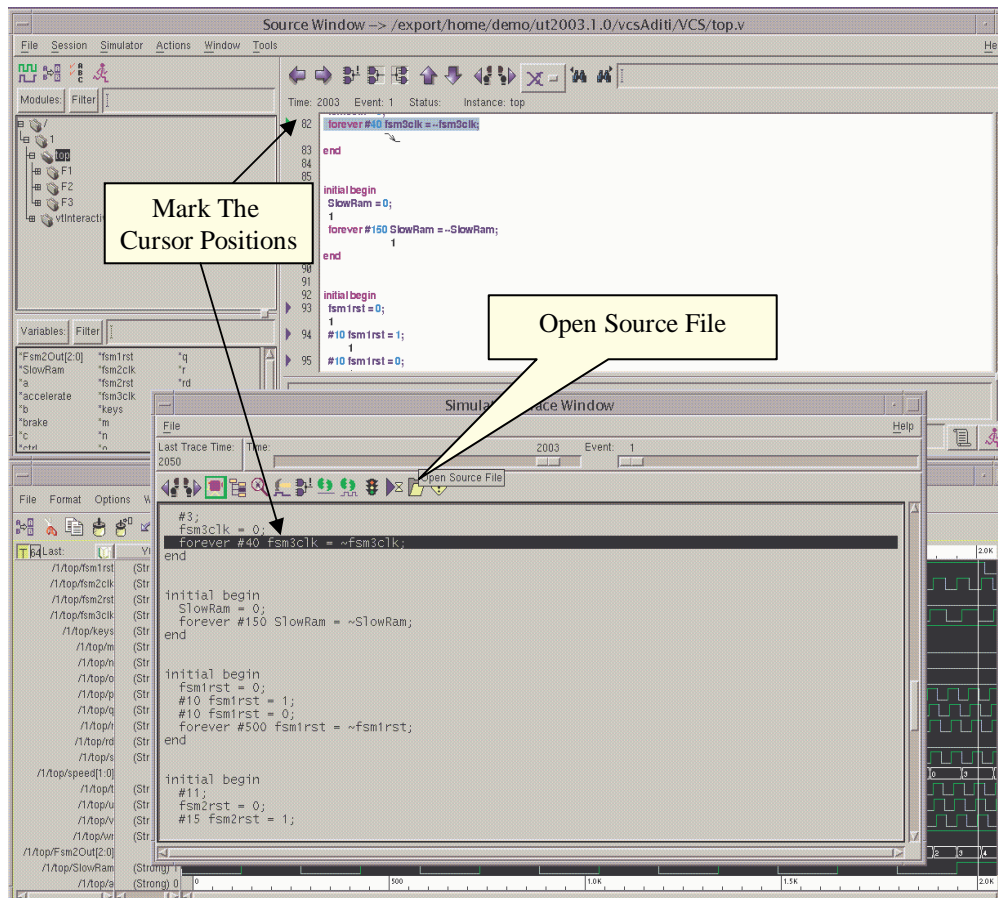
- To view the new changes in the value of the signal
- From the Source Code Window menu choose
- Window => Open Window - > Inspect Signal
- Select the signal and drag and drop it in the text area for the “Signal” in the “Signal Inspector” window
- Press “Update”
- The new value of the signal at the current time will be displayed

Trace Window



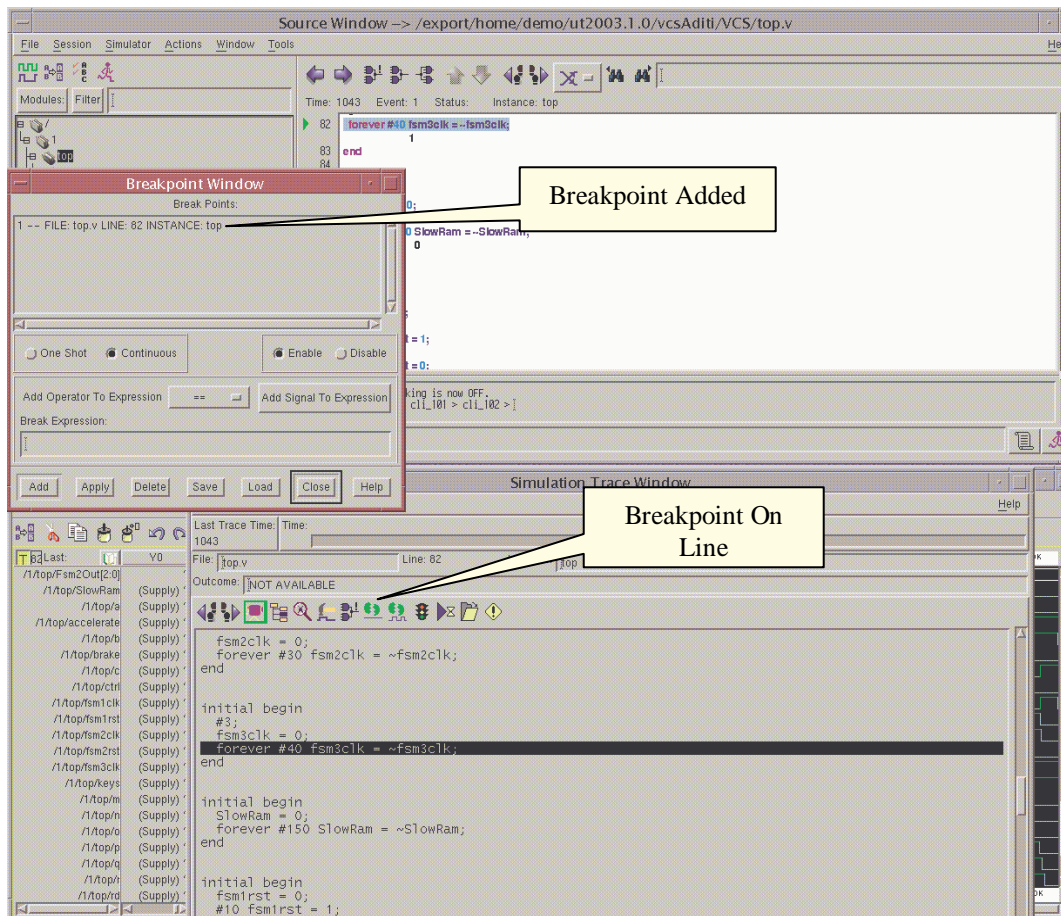
- “Simulation Trace Window” allows to move to next simulation point by using “Step Forward” button if you are at the last simulation time point
- Or to move backward in the past simulation time by using “Step Backward”
- To move forward in the past simulation use “Step Forward”
- If the simulator is running and last time point in simulation is reached clicking on “Step Forward” will advance the simulation one step further

Source & Trace Window Synchronization



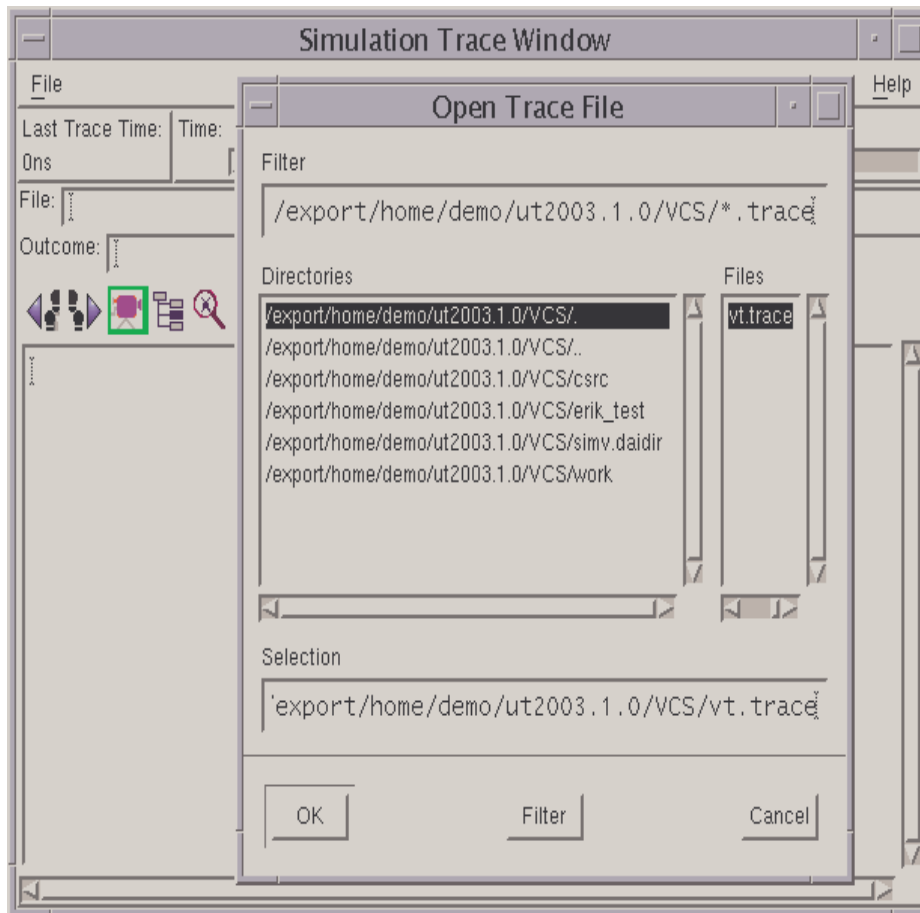
- To force the “Source Window” to be at the same point in simulation as “Trace Window” click on “Open Source File” button

Trace - Breakpoints



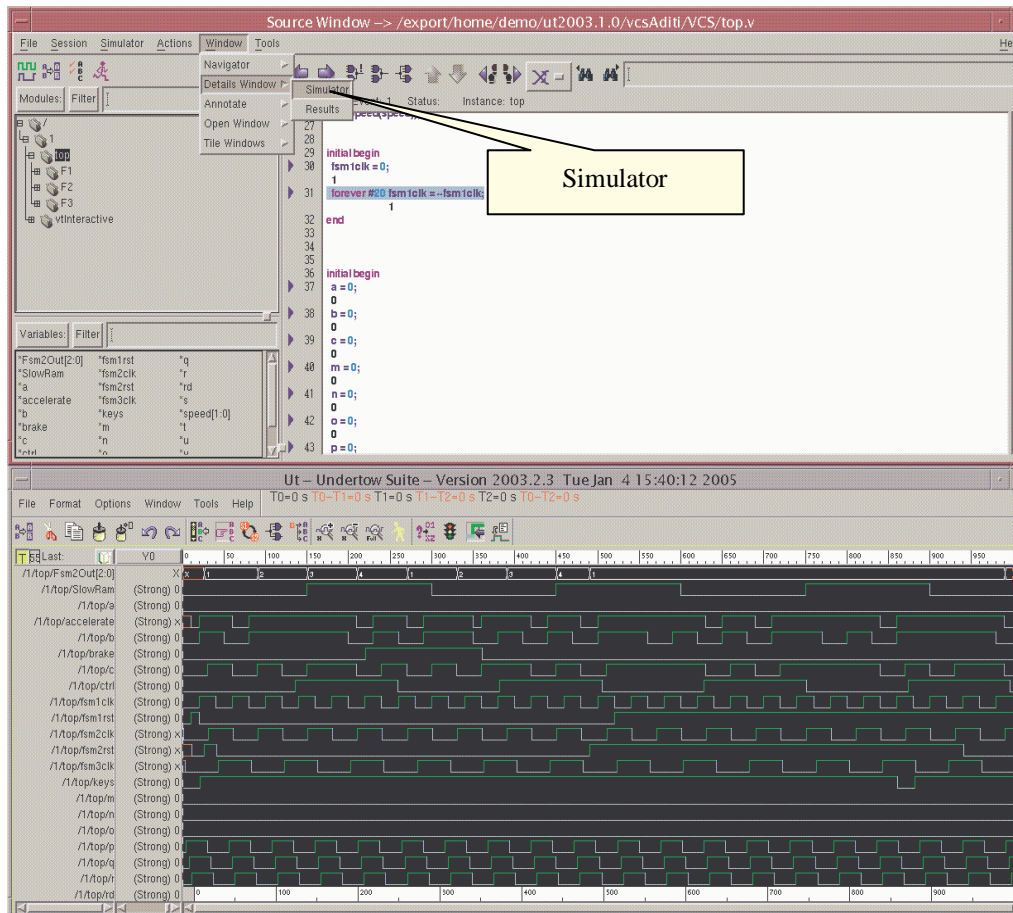
- To add the breakpoint in the “Simulation Trace Window” at the given cursor position
- Click in “Breakpoint On Line” button

Virtual Trace



- To view the trace file when the simulation is not running
- From the Simulation Trace Window menu choose:
- File => Open Trace File ...
- Select the desired “.trace” file and click “Ok”

Simulator Window



- To view the Simulator Window in the “Source Window”
- From the Source Window menu choose:
 - Window => Details
 - Window -> Simulator

Simulator Window



The screenshot displays the Veritools simulator interface. The top window, titled "Source Window", shows the source code for a Verilog module named "top.v". The code includes an initial block and a forever loop. A yellow callout box labeled "Simulator Window" points to the source code area.

```
Time: 999 Event: 1 Status: Instance: top
27
28
29 initial begin
30   fsm1clk = 0;
31   forever #20 fsm1clk = ~fsm1clk;
32 end
33
34
35
36 initial begin
37   a = 0;
38   b = 0;
39   c = 0;
40   m = 0;

```

Below the source code, an "INTERACTIVE BREAKPOINT @ ACTIVATED: 1020.000000" message is visible, followed by a list of command-line arguments: "cli_10 > cli_11 > cli_12 > cli_13 > cli_14 > cli_15 > cli_16 > cli_17 > cli_18 > cli_19 > I".

The bottom window, titled "Ut - Undertow Suite - Version 2003.03 Tue Jan 4 15:40:12 2005", shows a timing diagram. A yellow callout box labeled "Command Line Window For Simulator" points to the timing diagram area. The diagram displays various signals over time, including "Fsm2Out[2:0]", "SlowRam", "Accelerate", "Brake", "Ctrl", "Fsm1clk", "Fsm1rst", "Fsm2clk", "Fsm2rst", "Fsm3clk", "Keys", "M", "N", "O", "P", "Q", and "Rd".