What's new in ut2010.1.3

1. Expanded the ULTA mode to now include both analog signal data from analog simulators and digital data from digital simulators. Users can now speed up loading and displaying analog data by 3-4 times while at the same time reducing their memory foot print when loading and displaying signal by 3-4 times.
Users with mixed mode designs, that have both analog and digital data can now also speed the loading and displaying of signal data by 3-30 times while reducing their memory foot print at the same time by 3-30 times.

2. Added WGL and STIL file translators to the software distribution for vWave and VeritoolsDesigner. Users can now bring their WGL and STIL files into the vWave, while viewing their input/outputs in a schematic view and while also displaying the source code for their WGL and STIL files. Users can modify their WGL or STIL files to fix an issue, by selecting an editor right on the source code window, and then instantly see what effect this source code modification has on the resultant test vector waveforms.

Users can go to the visual-dft directory in the software distribution to find a readme.txt on how to set up and use the new WGL and STIL file translators.

What's new in ut2010.1.2

1. Released the ULTRA mode for digital designs. This update also includes a 3-30 times speed up of loading and displaying digital waveforms into vWave or VeritoolsDesigner from the simulation waveform data files. The memory footprint for loading and displaying waveforms is now also 3-30 times smaller.

NOTE: Users who want to use the ULTRA mode to speed up loading and reading data into vWave and VeritoolsDesigner must first obtain a license for ULTRA, listed on the license feature line as, "ut_ultra_feature". These licenses are provided at no cost to users who are currently on maintenance and will remain in effect while the user stays current on maintenance.

2. Added the ULTRA_PLUS mode of operation, which removes unconnected and redundant signals from the output simulator data. This can provide a many times speed up of the simulator while resulting in smaller waveform files, smaller by many times.

NOTE: Users who want to use the ULTRA_PLUS feature to speed their simulator speeds must first obtain a license for ULTRA_PLUS, the license lists this feature as the "ut_ultra_plus_feature".

Users can use both the ULTRA to speed up loading and displaying signal data, while at the same time using the ULTRA_PLUS feature to speed up their simulator.

3. New system commands were added to allow users running the VCS simulator to run three times faster when the user combined Verilog with SystemVerilog in their design. This will speed up any VCS simulation running Verilog and SystemVerilog by 3 times. This feature is provided at no cost to users who are currently on maintenance and will remain in effect while the user is current on maintenance.

4. Fixed issue with API and using double precision numbers so waveforms from these files will now look like analog and signals in these type of files can now be interpolated.

5. Fixed issue with vdump2 where the data sometimes would go out of scale.

What's new in ut2010.1.1

1. Fixed issue with API and using double precision numbers so waveforms from these files will now look like analog and signals in these type of files can now be interpolated.

What's new in ut2010.1.0

1. Completed the "ULTRA" feature, this makes the software 4-40 times faster when loading and digital displaying signals by allowing users to have a much more compact data base.

2. Added SUSE 11.2 support for 32 and 64 bit platforms

3. Updated User Guide ut2010.1.0 to indicate that based on testing that the fastest commands for VCS, when using Verilog with SystemVerilog are;

$dumpvars():
$vtDump;

This combination of commands gives simulation speeds that are about 2 ½ to 3 times faster, than using routines that are using the VPI system calls.

What's new in ut2008.1.4

1. Fixed hierarchically connected vector signal waveforms

2. Fixed hierarchical name listing for any signal

What's new in ut2008.1.3

1. Added major speed up to the Veritools VPI, PLI by removing callbacks for signals that are unconnected or do not change.

2. Added additional speeds ups by optimizing VPI code

3. Added SuSe 32 bit port

4. Added CentOS-5 both 64 bit and 32 bit ports

5. Added a libvtvpi_vcs.so port for Verilog only VCS

6. Fixed static declaration of memory file calls to work with VCS simulator.

7. Veritools work around for single +incdir+ command line option, use multiple +incdir+ command line options if user wants more than one +incdir+:

   +incdir+dir1 +incdir+dir2 +incdir+dir3

8. Built the PLI for the Aldec Riviera-PRO simulator

9. Fixed cosmetic spacing issue for vWave/Undertow for utf writers that display the module names too close together in the choose window, shows up when sub-modules have short names that are exactly the same length

10. Added support to utF API so utF files can go above 2147484148 bytes

What's new in ut2008.1.2

1. The schematic now makes room for updating blank values on component pins

2. Fixed dragging single items from the choose window to single line text areas such as the eye diagram window and the convert to digital window.

3. Added "Standard eye with clock signal" to the eye diagram window.

4. Fixed snap for eye diagram waveforms.

5. The new vdump executable is called vdump2. (A new ut executable is required to read the new vdump2 files.) It supports two new command line arguments:

-Z #chunks

This tells the vdump2 to make a 280 mode file using the specified number of chunks equivalent to +VTNUMCHUNKS in the PLI. The default is 1 which tells it not to make a 280 mode file.

-z #MB_per_chunk

This tells the vdump2 the size to use for a compression chunk in megabytes which is equivalent to +VTCHUNKSIZE in the PLI. The default is 16 which tells it to use 16MB per chunk.

6. Added support for making uncompressed fast files over 2GB in size with vdump2.

WHATS NEW IN 2008.1.1

1. Added support for modeltech fli in libvtvpivhpi_mt.so.

2. "Display Current Drivers" in the source window now uses the Expression evaluator to try to find the current driver for the signal.

3. Added several partial update strategies to the schematic window to keep it from slowing down the whole tool. Prior to this feature moving the cursor on the waveform window would be slow if a large schematic with many elements was displayed due to the speed of updating all of these elements.

4. Verified support for SV interfaces and SV modports.

5. Fixed highlighted nets on the schematic so they are retained when going up scope and down scope.

6. Decoupled module port names from the pins outside of the module so they can be used for selecting restricted nets on down scope in the schematic without affecting other features (highlight net, etc.)

7. Up scope in the schematic will now automatically expand nets that were previously highlighted.

8. Added Options -> Up scope, Show Whole Module to the schematic window. When toggled "on", the Up scope operation will show the whole schematic at the new scope.

NOTE: Up scope operations: Users can now select a net on a pin of any element going out of this module, and go up scope to see this module and pin and the connections to other gates and modules connected to this pin.

Toggling down the Option => Up scope, Show whole module will show the entire schematic for the up scope module and the selected net in the lower module will be highlighted in the up scope module.

Down Scope Operations: Users go down scope by double clicking into the black space inside of any module. If an outside pin on this module is selected, the down scope module will highlight the pin that was selected in the up scope module. If a module inside pin is selected, then the user will see only the down scope schematic for that selected pin and the logic connected to just that pin.

WHATS NEW IN 2008.1.0

1. Updated the VPI/VHPI to include MTI FLI interface.

2. Added latest parser to vtcom and VeritoolsDesigner

3. Added in trace back for Show Input Cone for schematics with no signal values.

4. Added in trace back for tracing from point A on schematic to point B, an instance name of schematic element.

5. **New PLI commands, modes:**

$vtVpiDumpflush;

$vtDumpSuppress(name), The "name" can either be a hierarchical module name or a defined module name.

$vtVpiDumpSuppress(name), The "name" can either be a hierarchical module name or a defined module name.

$vtDumpsuppress/$vtVpiDumpsuppress, calls must be made before the call to $vtDumpvars/$vtVpiDumpvars in order to have any effect.

Using the new +VTCOMPRESS280 mode to make compressed files.

This file format divides the data into a fixed number of separate chunks. +VTNUMCHUNKS<number> controls the number of chunks to use.

Only the first $vtDumpvars() call will be divided into separate chunks. Subsequent $vtDumpvars() calls will each use one new data chunk. +VTNUMCHUNKS10 is the default. +VTCHUNKSIZE<number> can be used to set the size of each uncompressed data chunk in MB. +VTCHUNKSIZE16 is the default (16MB). Examples:

%ncsim -f ncsim.args +VTCOMPRESS280

%ncsim -f ncsim.args +VTCOMPRESS280 +VTNUMCHUNKS200

%ncsim -f ncsim.args +VTCOMPRESS280 +VTNUMCHUNKS1000 +VTCHUNKSIZE4