Tutorial for VeritoolsVerifyer, SystemVerilog Assertions

VeritoolsVerifyer

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Tutorial for SystemVerilog Assertions

To run the VeritoolsVerifyer, do the following steps:

- % cd /flexlm and launch License Manager
- % Run lmgrd for VeritoolsVerifyer license
- % cd /(distribution directory)/examples/dma_assertions
- % run_ut_batch_new

(Script is: ut -iv -sysver -source -sigfile vt.dump)

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Start the VeritoolsVerifyer, by selecting the **Tools** menu item as shown above.

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The VeritoolsVerifyer window contains an Icon Bar near the top under the Menu Items, a Heirarchy area in the Upper Right, the window holding the assertions for the selected module, and the Bottom Window displays the text for the selected assertion. Selecting the + in the Module Window opens the modules below this level (see next screen.)

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E 1_dna_dunp_fast	p0within p1within p2within	A

By selecting the Name of the Module, the assertions in that module are displayed in the Assertion List Window.

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property pWITHIN (ov,ama_reqv,aata_accepteav,aone_amav) ;	- Iî
go, dma_req, data_accepted, done	_dma) ;	
<pre>@ (posedge clk)(go => ((\$rose(dma_r)</pre>	eq) ##(1) ((##[1:4] data_accepted) [* 2])) within f	fire
endproperty	▶	
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Selecting an Assertion in the Assertion List Window, displays the Assertion Text in the bottom window. In the screen below, the assertion **p1within** (background is highlighted) is selected:

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<pre>plwithin : assert property pHITHIN(go1,dma_req1,data_c property pHITHIN (go, dma_req, data_accepted, done_dma) ; @ (posedge clk)(go => ((\$rose(dma_req) ##(1) ((##[1: endproperty</pre>	accepted1,done_dmal) ; 4] data_accepted) [* 2])) within first_match((##[0:9] done_dma)))); }	

Next, use the **Evaluate All Assertions In Module** icon.

Note: All assertions at this level and all modules below this level will be evaluated.

Also, this will color code the hierarchy, and if even one assertion fails at this level or below this level, the entire hierarchy will be color coded **Red**.

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plwithin : assert property pWITHIN(gol,dma_reql,data_d	accepted1,done_dma1) ;	
property pWITHIN (
<pre>@ (posedge clk)(go => ((\$rose(dma_req) ##(1) ((##[1:</pre>	:4] data_accepted) [* 2])) within first_match((##[0:9] done_dma))));	
endproperty		
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After assertions are evaluated, the assertions will turn Yellow if Vacuously True, **Green** if the assertion Passes and **Red** if it Fails or if it is still pending past the end of simulation. The next step is to press the **Display Assertion Results** icon. This displays the assertion result waveform in the waveform window, as shown above. A low going pulse indicates the assertion failed, a high going pulse indicates the assertion passed. The leading or falling edge of this pulse indicates where the assertion started.

Note: The cursor is automatically placed on the leading edge of the Assertion Result Pulse, which is a low going pulse if the assertion failed, and a high going pulse if the assertion passed.

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plwithin : assert property pWITHIN(gol,dma_reql,dat property pWITHIN (go, dma_req, data_accepted, done_dma) ; © (posedge clk)(go => ((\$rose(dma_req) ##(1) ((## endproperty	ta_accepted1,done_dma1) ; #[1:4] data_accepted) [* 2])) within first_match((##[0:6] done_dma))));

After evaluating the assertion and displaying the result, the assertion text is automatically color coded, **Green** for the part of the assertion that Passes evaluation, **Red** for the part that does not pass evaluation.

Note: the assertion is evaluated only when the T0 cursor is on the leading edge of the assertion result pulse, which is automatically done when you press the **Display Assertion Result** icon.

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go, dwo_req, dato_accepted, dome_dma) ; (opsedue clk)(ao => ((\$rose(dwo_req) #W(1) ((##[1:4] data accepted) [* 2])) within first match((##[0:6] dc	one dma))));		- 88
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Next, click the **Display Assertion Timing with Components** icon. See above.

Note: the assertion timing signal indicates when the assertion is inactive, when it goes active and the latest possible time when it goes to a True or Fail condition.

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plwithin : assert property pWITHIN(gol,dma_reql,dat	a_accepted1, done_dma1) ;	2
property pWITHIN (
go, dma_req, data_accepted, done_dma) ; (posedep_slk)(ap_l=>_((\$reso(dma_reg) ##(1)_((##	[1,4] data accorted) [+ 21)) within first match((##[0,6] dama dama)))).	l
endpropertu	[1.4] dutu_uccepted/ [* 2]// wrthin /irst_Mutch((##[0.0] done_dMu////	l
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To fix the error condition causing the assertion not to pass, look at the **Red** portion of the assertion. The condition causing the assertion to fail is the parameter defining the requirements for this signal. In this case, **dma_done** is required to come true within clocks 0 through 6. But as seen in the waveform viewer, it comes true on clock 7.

To fix this assertion, press the <u>Edit Assertion</u> icon, which turns the assertion text window into an "edit/what if" window. After pressing the <u>Edit Assertion</u> button, the text in the "edit/what if" window will no longer be color coded as shown in the next screen shot.

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⊟ 1_dna_dunp_fast Le <mark>dina_test</mark>	pOwithin (Op Of 150 Ou) pluithin (Op 1f 140 Ou) p2within (Op 1f 140 Ou)
(go) => ((\$rose(dma_req) ##1 (##[1:4] data_accepted)[* (first_match(##[0:6] done_dma))); endproperty: pWITHIN	2]) within

Replacing the number 6 with a number greater than 6 will cause this assertion to **Pass**.

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<pre>B 1_dna_dunp_fast</pre>
(go) => ((\$rose(dma_req) ##1 (##[1:4] data_accepted)[*2]) within (first_match(##[0:9] done_dma))); endproperty: pMITHIN

After editing this assertion, run **<u>Retest</u>**, the icon to the immediate right of the <u>**Edit Assertion**</u> icon:



This action will retest the modified assertion code.

The Retest icon is only active when in Edit mode (when the **Edit Assertion** icon is depressed. This allows users to modify and retest this assertion as many times as necessary.

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Notice, after clicking <u>Retest</u>, if the assertion passes, the assertion timing signal will go inactive, active, pass, the assertion result will now show a high going pulse, and the assertion in the assertion list window will turn green. After the assertion passes, the user can then commit the modified code.

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(posedge c]k)		Ī
(go) =>		
<pre>((\$rose(dma_req) ##1 (##[1:4] data_accepted)[* (first match(##[0:9] done dma))):</pre>	2]) within	
endproperty: pWITHIN		ij
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To commit, click the **<u>Commit Edited Assertion & Reparse</u>** icon as above:

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a test.p1within(50) fast/dma_test/gal Ima_test/dma_test/gal ia_test/dana_test/dka o_fast/dma_test/ckk Vdma_test.p1within	active inactive	50n 100n		in	200n	2500
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Note: after pressing **<u>Commit Edited Assertion & Reparse</u>** a dialog box will ask if you wish to overwrite your source file for the assertion code.

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dna_test	pluithin
plwithin : assert property pWITHIN(gol,dma_reql,da	ta_accepted1,done_dma1) ;
property pWITHIN (
go, dma_req, data_accepted, done_dma) ;	
<pre>@ (posedge clk)(go => ((\$rose(dma_req) ##(1) ((##</pre>	<pre>#[1:4] data_accepted) [* 2])) within first_match((##[0:9] done_dma))));</pre>
endproperty	

Notice once the code is committed and reparsed, dma_done has changed from **Red** to **Green**, indicating the assertion now passes.

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go, dma_req, data_accepted, done_dma) ;				
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If there is a Red Downward Arrow in the assertion timing waveform (as shown above) it indicates this assertion has unique, independent execution threads. To display the unique, independent execution threads, select (click using left mouse button) the timing waveform (gray highlight, as shown above). Then press Options (pull down menu) -> and click **Show Threads for Selected Timing Waveform**.

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p1with proper go @ (pos endpro	<pre>plwithin : assert property pWITHIN(go1,dma_req1,data_accepted1,done_dma1) ; property pWITHIN (go, dma_req, data_accepted, done_dma) ; (posedge clk)(go => ((\$rose(dma_req) ##(1) ((##[1:4] data_accepted) [* 2])) within first_match((##[0:9] done_dma)))); endproperty</pre>									

The heirarchy and assertion windows are replaced by the above windows: the **Selected assertion timing** window, and the **Next thread generator** window.

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plwith proper go ⊚ (pos endpro	in : assert pr ty pWITHIN (, dma_req, dat edge clk)(go perty	operty pWITH a_accepted, => ((\$rose(d	IN(go1,dma_re done_dma) ; ma_req) ##(1)	eq1,data_accep ;) ((##[1:4] c	oted1,done_dr data_accepted	na1) ; I) [* 2])) wi	thin first_mat	ch((##[0:9]	done_dma))));	

Next, select the unique independent execution threads that you wish to display in the waveform display window. Click-and-hold with the left mouse button, and slide over the threads you wish to display. If you wish to select individual threads, select (left click) individually.

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Pressing the **Display Thread** button will display the selected threads in the waveform window. Notice within the threads shown, are additional unique independent execution threads, as shown by the downward pointing **Red** arrow, in the new assertion timing signals. This allows you to denest all of the unique independent execution threads in any given assertion.

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st.p1within{50'##6}	active	inactive	active			fail		
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st.p1within{50'##4}	active	inactive	active		fail			
st.p1within{50'##3}	active	inactive	active		fail			
st.p1within{50'##2}	active	inactive	active	fai	11			
st.p1within{50'##1}	active	inactive	active	fail				
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The above waveform window displays all the unique independent execution threads along with the timing signal for this assertion, the result signal for this assertion, and the signal components for this assertion.

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Selected assertion timing:											
Jna_test.p1within{503											
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										7	
	Display Thr	read		Display	Thread & Local	Yariables		Car	ncel		
plwith proper ga © (pos endpro	<pre>plwithin : assert property pMITHIN(go1,dma_req1,data_accepted1,done_dma1) ; property pMITHIN (go, dma_req, data_accepted, done_dma) ; @ (posedge clk)(go => ((\$rose(dma_req) ##(1) ((##[1:4] data_accepted) [* 2])) within first_match((##[0:9] done_dma)))); endproperty</pre>										

To return to the assertion heirarchy window, click the **<u>Cancel</u>** button.

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To see Coverage information, select the **Options** pulldown menu, then press **Coverage** (as shown above) to get the sub menu (next screen).

Note: System 44 Applications Places System	🕹 🙆 🗾						4 3) 📑 🖳	Tue May 17, 9:52 AM	demo
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Click Collect Coverage Data For All Assertions as shown above.

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This opens the coverage window, which shows the counts of each assertion: **Passes**, **Fails**, **Vacuously True** or **Pending** at the end of execution.