Every engineer has a PC on their desk. Learn how engineers can use their native Windows PC to accelerate their design and debug efforts using the tools from Veritools, all at a much lower costs than their current tools. All of Veritools software will run exactly the same on either the PC in native Windows or on any of the most popular variations of Linux, allowing designers to switch to whatever platform that gives them the most productivity at the lowest costs.

MIXED MODE DESIGNS Learn how **vWave,** currently the only EDA software with complete features for both analog and digital designs, can greatly accelerate your debugging for designs that have both analog and digital elements.

RTL SOURCE CODE DEBUGGING Learn how **VeritoolsDesigner**, which includes source code debugging for Verilog, SystemVerilog and VHDL, and automatic State diagram extraction along with RTL/Gate schematic extraction and display can not only speed up your design process, but will significant lower your EDA tools costs.

SVA DESIGN VERIFICATION Learn how the **VeritoolsVerifyer, with the built in Stand along SystemVerilog Simulato**r, can speed up your design and verification efforts by many 100s of times. The “What if” window, allows users to see the exact part of the assertion that is failing evaluation, and then allows users to modify this code and rerun this one assertion in seconds, an operation that could take many hours if not days with their digital simulator. This software also automatically records design coverage at the same time.

All of these tools will run identically on a PC in native Windows or on Linus and are also available as libraries for use with other EDA tools.

These tools have Perl and now Python scripting built in, and **can run in a batch process** without bringing in the GUI **for automatic design testing**.